FPGA-Based Farsi Handwritten Digit Recognition System

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***Abstract* - A new method for feature extraction based on FPGA (Field Programmable Gate Arrays) implementation is proposed in this paper. The specific application is offline Farsi handwritten digit recognition. The classification is based on a simple two layer MLP (Multi Layer Perceptron). This method of feature extraction is appropriate for FPGA implementation as it can be implemented only with addition and subtraction operations. The proposed method is used to extract the features from normalized 40×40 pixel handwritten digit images from Standard Hoda database. Exprimentally results showed that the proposed system achived about 96% accuracy. Overally the system is simple, more accurate and less complex than the other similar systems.**

Keywords: FPGA, Handwritten Digit Recognition, VHDL, Digit, MLP, Feature Extraction.

I. INTRODUCTION

Automatic (machine) recognition, description, classification, and grouping of patterns are important problems in a variety of engineering and scientific disciplines such as biology, psychology, medicine, marketing, computer vision, artificial intelligence, and remote sensing [1]. The most commonly used family of neural networks for pattern classification tasks is the feed-forward network, which includes multilayer perceptron and Radial-Basis Function (RBF) networks [1]. Generally, a pattern recognition system is implemented using software technology. However, the speed of software-based implementation is low, and software-based implementation relies on computer and is not suitable for using in the environments where high portability is needed [2]. FPGAs are a form of programmable logic, which offer flexibility in design like software, but with performance speeds closer to Application Specific Integrated Circuits (ASICs). FPGAs can be reconfigured repeatedly, making them ideal prototyping tools for hardware designers [3].

In this paper, a new method is introduced for implementation of recognition systems on FPGA chip. Our specific problem of interest is recognition of handwritten Farsi digits.

In recent years, many researchers have worked towards effective algorithms for Optical Character Recognition (OCR) of Persian and Arabic texts [4-12]. However, with growing applications of Field Programmable Gate Arrays (FPGAs), no effort is reported to implement these algorithms on hardware chips [13].

Several obstacles had to be overcome in order to implement this recognition problem on an FPGA. Only digital images of the digits can be synthesized by FPGA. Therefore, at first the images should be quantized. Quantization reduces the accuracy of the system.

Another problem is the high number of division and square operations and big multipliers that are used in implementation of recognition systems. Since these operations are not embedded in FPGA chips, their implementation requires a significant portion of FPGA resources, thereby reducing the speed of the recognition process.

In this paper a new combined method for feature extraction of handwritten Farsi digits is introduced. This method has some advantages: 1) we need only low bit adders for implementation of the feature extraction part. 2) We use only integer calculation. 3) All extracted features are integer.

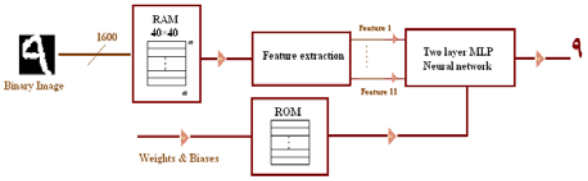
In this paper we use offline learning method. Offline training occurs when learning occurs on a general-purpose computing platform before the trained system is implemented in hardware [14]. MATLAB [MathWorks] has become the preferred language of computing for researchers [20]. We have used Matlab Neural network library for training our neural network system before the trained system is implemented in hardware [21]. A simple MLP classifier with only a few neurons in the hidden layer was utilized for classification, thereby economizing in the hardware resources.

This paper is organized as follows: Section 2 represents the block diagram of an offline Farsi handwritten digit recognition system. Section 3 explains method of feature extraction in two parts. Section 4

introduces specifications of the proposed MLP neural network classifier. Section 5 presents the method of sigmoid activation function implementation. Section 6 presents the Result and discussion about results, and finally section 7 concludes the paper.

II. BLOCK DIAGRAM

The block diagram of an FPGA implementation of



Farsi handwritten recognition system is shown in figure1. The feature extraction and classifier part of this block diagram is explained in section 3 and section 4.

Figure 1. The block diagram of an offline Farsi handwritten digit recognition system.

III. FEATURE EXTRACTION METHOD

The method of feature extraction is combined of two approaches. These approaches are explained below.
Eleven features are extracted by using this method of feature extraction. All of extracted features are integer and could be implemented with only add and subtract operation on FPGA. These approaches executed parallel on FPGA.

We implement this method with VHDL language. We use ten parallel processes for implementing this method (as shown in figure 2).

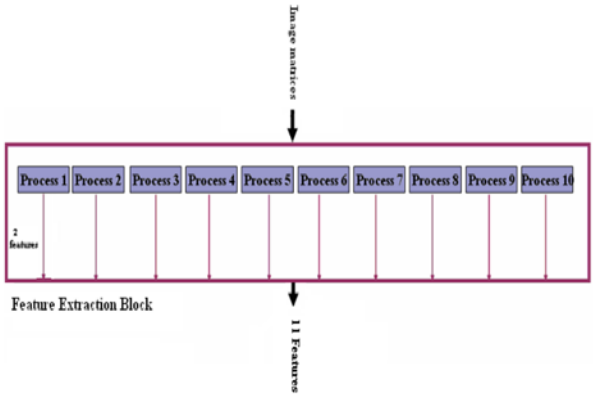


Figure 2. The block diagram of feature extraction block.

A. Statistical Approach

A statistical approach is used for representing the spatial distribution of the pixel values of binary images to compare number of white pixels on the upper and lower halves and also left and right halves of the digit image. This approach is usually used for typing digits. Normally in typed digits, on similar font and size, some typed digits have left halves bigger than right halves. some digits have bigger right halves, some digits have similar left halves and right halves, also some digits have upper halves bigger than lower halves, some digits have lower halves bigger than upper halves and some digits have lower halves similar to upper (as shown in Figure 3.). Some digits have 2 form of writing like 4 and 6.

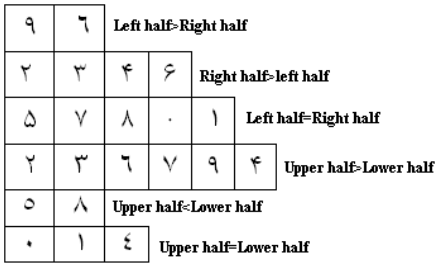


Figure 3. Compare left halves and right halves and upper halves and lower halves of digits.

This feature is an appropriate feature for pattern recognition of typed digits but in handwritten digits it is useful when combined with other features. Because in normalized handwritten pictures, the middle of the picture and the middle of the digit are not compatible (as shown in Figure 4.).

This feature is simple for implementation on FPGA. Only the white pixels in different areas of the image (top, and middle of the picture, and right and left of the middle of the picture) need to be counted.

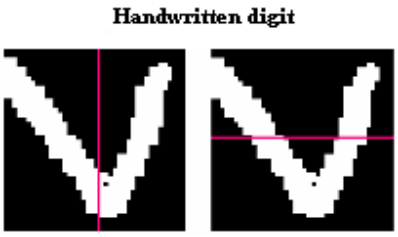


Figure 4. Handwritten digit image

This feature only requires the addition operation for FPGA implementation. Process 1 of VHDL program that is shown in figure 2 has used for implementation of this section of feature extraction method.

Two features are extracted by using this method of feature extraction.

B. The Number Of Intersections

This feature extraction method has two parts (1) Count the number of intersections along middle vertical ray [22]: This feature is useful for dividing digits to some groups. Some digits have two intersections along middle vertical ray. Some digits have one intersection along middle ray, and some digits have more than two intersections (shown in Figure 5). This feature is useful when combined with other extracted features [15].
Process 2 of VHDL program that is shown in figure 2 has used for implementation of this section of feature extraction method.

One feature is extracted by using this method of feature extraction.

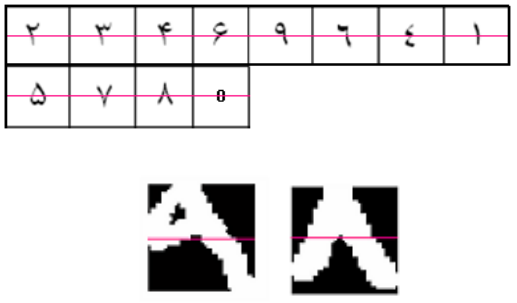


Figure 5. Count the number of intersections along horizontal ray of handwritten and typed images.

(2) We divide the pictures to eight sections: Four vertical and four horizontal sections.
We count horizontal intersections along ten horizontal equi-spaced rays (in horizontal sections) and vertical intersection along ten equi-spaced vertical rays (in vertical sections) in each section.
This method is appropriate to separate some similar digits like 2 and 3 (as shown in Figure 6). This feature only requires the add operation for FPGA implementation.
Process 3-10 of VHDL program that are shown in figure 2 has used for implementation of this section of feature extraction method.
Seven features are extracted by using this method of feature extraction.

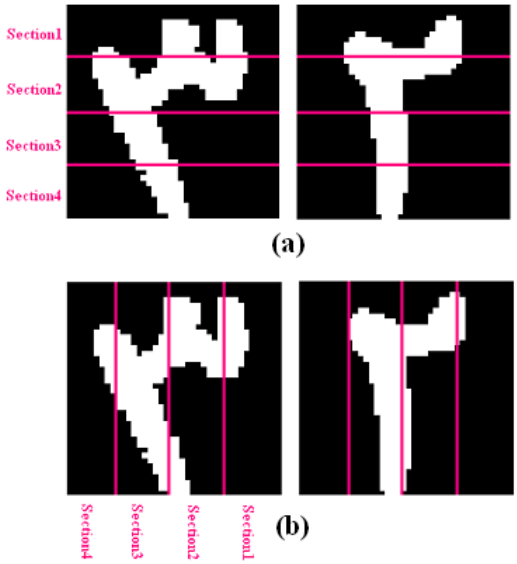


Figure 6. Pictures are divided to four horizontal and four vertical sections.

IV. PROPOSED MLP NEURAL NETWORK CLASSIFIRE

MLP neural network is one of the most common families of neural networks for pattern classification tasks.
In this project we used an MLP neural network with one hidden layer (shown in Figure 7). The specifications of proposed classifier are shown in table I.

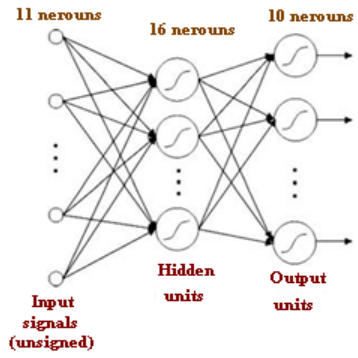


Figure 7. Multilayer perceptron. For simplicity, the bias terms are not shown [20].

In this paper we used 18000 normalized (40×40) binary images of standard Hoda database [12] for training the neural network and 2000 normalized (40×40) binary images for testing the neural network.
In this paper we use offline learning method. We used Matlab for training the neural network and obtaining weights and biases for implementation on FPGA. We save weights and biases as a constant in FPGA ROM (as shown in figure1).

TABLE I. Specifications of proposed MLP neural network classifier

Number of neurons in input layer	Number of neurons in hidden layer	Number of neurons in output layer	Activation Functions
11	16	10	'logsig' 'logsig'

Figure 8 approximately represents the recognition rate of the neural network versus increasing the number of nerons in hidden layer.

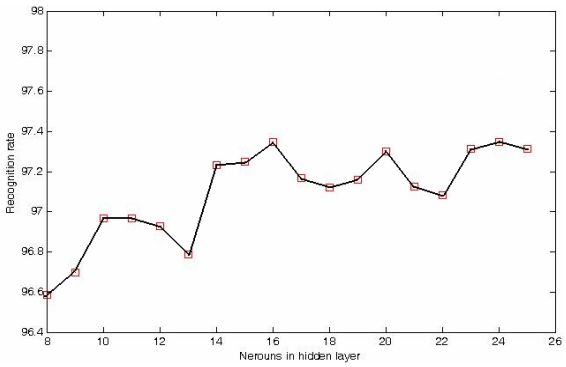


Figure 8. Recognition rate versus increasing nerons in hidden layer.

Figure 9 shows the block diagram of requirement parts for implementation of MLP neural network classifier.

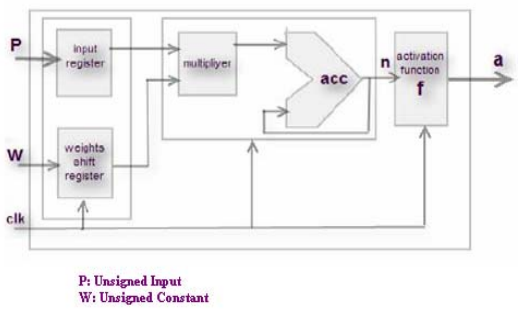


Figure 9. The block diagram of requirement parts for implementation of MLP neural network classifier.

We used Serial by Parallel Booth algorithm for implementation of multipliers and we used Carry Ripple Adder method for implementation of adders (as shown in figure 10).

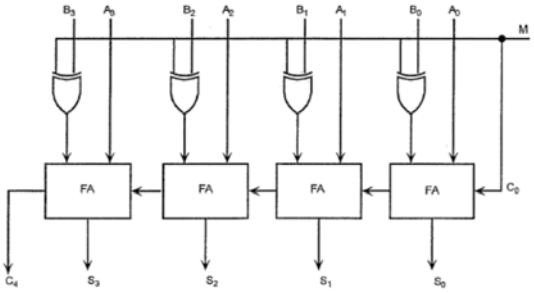


Figure 10. Carry Ripple Adder Block Diagram [16].

Implementation of activation function is explained in section 5.

V. SIGMOID ACTIVATION FUNCTION IMPLEMENTATION

For implementing our activation functions by FPGA, we use Piece-Wise Linear Approximation. This method has sufficient precision for our implementation.

A. Piece-Wise Linear Pproximation (Pwl)

This approach for implementing the sigmoid function consists of a linear approximation of logsig function defined by (1) and its diagram is shown in figure 11.

$$\theta(v) = \frac{1}{(1+e^{-v})} \tag{1}$$

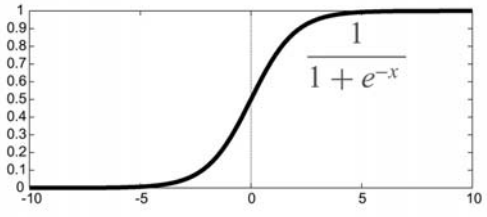


Figure 11. Logsig diagram.

The formal mathematical representation of this approximation is expressed by (2) **[**17**]**.

$$\theta(v) = \begin{cases} 1 & for \quad v \geq 4 \\ 0.0625v + 0.75 & for \quad 0 < v < 4 \\ 0.5 & for \quad v = 0 \\ 0.0625v + 0.25 & for \quad -4 \leq v < 0 \\ 0 & for \quad v \leq -4 \end{cases} \tag{2}$$

Figure 12 shows the 5-piece graph of this linear approximation sigmoid function.

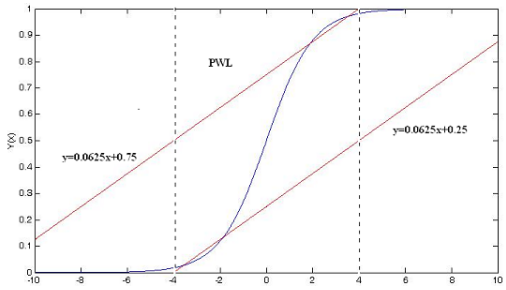


Figure 12. Implementation of PWL approximation of logsig function.[17]

VI. RESULT AND DISCUSSION

The results of Matlab simulation for each feature extraction method alone are shown in table II . The result of matlab simulation after combining two methods is shown in table III.

TABLE II. The results of Matlab simulation for each of feature extraction method alone

Method 1 Statistical approach	Recognition percentage of system for testing data	Number of neurons in hidden layer of classifier
	90.18%	10
Method 2 The Number Of Intersections	Recognition percentage of system for testing data	Number of neurons in hidden layer of classifier
	94.43%	9

TABLE III. The result of matlab simulation (After combined three method of feature extraction)

Recognition percentage of system for training data	Recognition percentage of system for testing data	Number of neurons in hidden layer of classifier
97.3%	97%	16

The off-line Farsi handwritten digit recognition system was implemented by VHDL language. This system is synthesized by Xillinx ISE 10.1 and simulated with Modelsim SE 6.3F. Simulation result for an example handwritten digit is shown in figure 13. Weights and biases that are obtained from Matlab simulation are floating point. In order to economize hardware resources, weights and biases of the neural network are expressed using fixed-point numbers (one number of decimal) in the FPGA-based implementation. Therefore, recognition rate in FPGA-based implementation is slightly lower (about one percent) than that of Matlab simulation result.

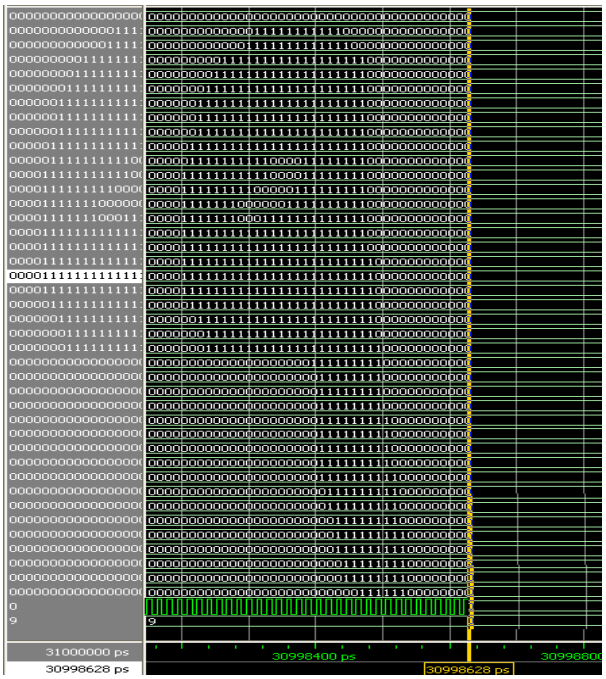


Figure 13. Simulation result for an example handwritten digit

We use xc3s1400an-5-fgg676 chip of Spartan3A series from Xillinix manufacture because of its appropriate number of embedded multipliers and enough RAM. The architecture and features of this chip are shown in figure 14 and table IV.

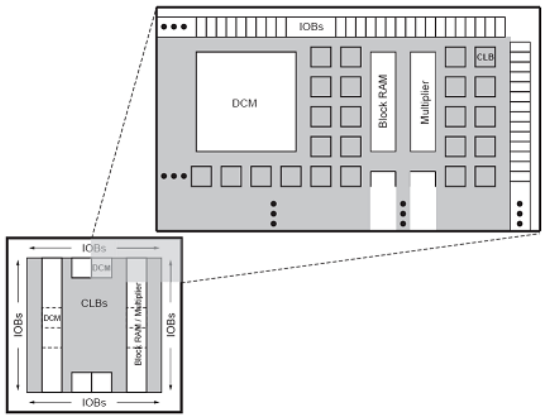


Figure 14. The architecture of Spartan3AN series FPGA chip [18].

TABLE IV. Feature's table of XC3s1400an-5-fgg676 chip [19].

Device	System Gates	Equivalent logic cells	CLBs	Slices	Distributed RAM bits	Block RAM bits	Embeded multipliers	DCMs
XC3S1400AN	1400K	25,344	2816	11,264	176K	576K	32	8

The result of FPGA implementation is shown in table V. This system is more accuracy than other proposed digit recognition system like [2].

TABLE V. Experiments result of function simulation of FPGA system and PC-based system

Approach	Recognition rate
(PIV , 2.16G CPU, 4G RAM, WinXP operating system)	≈ 97%
FPGA (system clock is 112MHz)	≈ 96%

VII. CONCLUSIONS

In this paper, we combined two approaches of feature extraction methods. These methods are executed parallel on FPGA. By implementation of this method, we obtained an appropriate accuracy in FPGA-Based Farsi handwritten digit recognition system. A simple MLP classifier with only a few neurons in the hidden layer was utilized for classification. By implementation of this method, we obtained more accurate system than hardware handwritten Latin recognition system.

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