A Highly Stable Millimeter Wave Low Noise Amplifier in 130nm CMOS Technology

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Abstract — The design of a 60 GHz four-stage cascaded low noise amplifier (LNA) is presented in this paper. By using proper microstrip transmission lines in the gate and source of the common-source transistor, high stability factor and low noise figure are obtained simultaneously. The proposed LNA is designed in 130nm CMOS technology and simulated using ADS software employing accurate models for both transistors and microstrip lines. The simulation results show a 14 dB gain and less than a 4 dB noise figure at 60 GHz. The stability factor (K) of the designed LNA is more than 10 in hole of the desired bandwidth.

Keywords – CMOS, Millimeter Wave, Low Noise Amplifier (LNA), Microstrip line, Stability

I. INTRODUCTION

The growing interest in millimeter-wave transceivers for consumer, radar and imaging applications has motivated work on various CMOS building blocks operating at 60 GHz and beyond [1]. Low noise amplifier is an essential component in the millimeter wave front-end transceiver. However historically, the design of LNAs in the 60 GHz band was based on compound semiconductors due to their very high unity gain frequencies, Nowadays CMOS technology is expected to enable low-cost mm-wave applications [2].

Numerous circuit and transceiver techniques in millimetre wave band have appeared in the literature [3]–[8]. [3] presented a millimeter-wave three-stage common source LNA in 130nm CMOS technology, using CPW transmission lines, which achieved a gain of 12, a NF of 8.8 dB and dissipated 36mW from a 1.5V supply. A 60GHz low power, low voltage LNA using forward body bias, was fabricated in 90nm CMOS process was presented in [4]. [8] reported a Current-Rused Cascade Amplifier (CRCA) in 90nm CMOS process and achieved a peak gain of 12 dB and a 6.9 dB NF at 51GHz while dissipating the DC power of 7.7mW. The designed current-reused LNA comprises two stacked common source amplifiers with the same dc current for each stage to enhance the power gain.

In this paper the design of a 60GHz four-stage LNA in 130nm CMOS is presented. In order to obtain precise results, accurate models of transistors and transmission lines at millimeter wave frequencies are used [8], [9]. To obtain the simultaneous optimum noise figure and stability performance, specific matching networks in the input of each stage and degenerating inductors in the source of transistors have been used.

II. AMPLIFIER DESIGN

A. Design of the Single Stage

Figure 1 shows the single stage of the designed LNA. The transistor’s gate width is chosen 31.7 μm for optimum noise figure and gain performances.

In order to minimize the noise figure of the LNA, the impedance seen by the gate of the transistor, have been equal to the optimum noise impedance of the transistor by using a matching network. This matching network is designed by using TLg as a short stub in the gate of the common source transistor.

Figure 1. Single Stage of the Proposed LNA.

In the proposed LNA, TLS plays an important role on the power gain, stability factor and noise figure of the...
LNA. Figures 2-4 show variations of these parameters versus frequency for four inductance values of TLS for a single stage of the LNA.

As can be seen, for LS less than about 10pH the stability factor is less than unity and the amplifier is unstable. It is clear that LS decreases power gain and increases stability. Also noise figure is minimum for LS=30pH. Therefore, LS=30pH is selected for minimizing noise figure and as a tradeoff between power gain and stability.

B. Transmission Line Model

IC fabrication technology is suitable for transmission lines of planar structures. As compared to coplanar waveguides (CPW), microstrip lines have a higher effective inductance per unit length and more flexibility in connection. Its ground plane also shields signal paths from lossy substrate. The microstrip lines are therefore chosen in this work for matching elements [9].

In 0.13 μm CMOS technology, the microstrip line structure appears as in Figure 6, which consists of the top metal layer (M8) as the signal stripline and the first metal layer (M1) as the ground plane. A viable model shall include both the dielectric parameters of relative permittivity εr, thickness H, and loss tangent (TanD), and the parameters of strip line thickness T, and metal conductivity [9].
Figure 7. Setting of microstrip substrate and microstrip line in ADS

Modeling of the structure in Figure 6 has been successfully put into practice in these components. Figure 7 shows the MSUB component in ADS simulator with the two adjusted parameters: The $\varepsilon_r$ and TanD values are set to 4.8 and 0.02 to match with the practice [9].

C. Transistor Model

The small signal model of a MOS transistor used for simulation of the proposed LNA is shown in figure 8 [10],

$$G_m = g_m \cdot \exp(-j \omega \tau)$$

Figure 8. Small Signal model of a MOS transistor used for simulation of the proposed LNA

Scalable model of MOS transistor at millimeter-wave. The scalable circuit elements of Figure 8 against gate width of the transistor, W, in $\mu$m have been calculated in [10] using measured S-parameters. The model values for $20 \mu$m < W < $80 \mu$m are as follows [10]:

$$r_{gs} = \frac{688}{W} - 2.5(\Omega)$$
$$C_{gs} = 0.96W - 1.6(fF)$$
$$C_{dgs} = 0.96W + 0.7(fF)$$
$$C_{ds} = 0.43W + 0.27(fF)$$

This model has been verified for 10 GHz < f < 100 GHz [10]. The model parameters for W=31.7$\mu$m are extracted as follows:

$$r_{gs} = 19.20 \ \Omega, \ C_{gs} = 28.83 \ fF, \ C_{dgs} = 11.48 \ fF, \ C_{ds} = 13.90 \ fF, \ r_{ds} = 236.54 \ \Omega, \ g_m = 20.19 \ mS, \ \tau = 828.02 \ \mu s, \ G_m = 20.19 . \exp(-j8.28 \times 10^{-13} \omega) \ mS.$$  

III. PROPOSED AMPLIFIER

Figure 9 shows the schematic of the proposed LNA. By cascading four stages the final design achieves a 14 dB gain. In order to make the design modular, similar stages are used in cascade. The amplifier parameters in each stage are subsequently re-optimized to achieve design goals.

Figure 9. Schematic of the proposed LNA.

Figure 10 depicts the simulated S-parameters of the proposed LNA from 50 GHz to 70 GHz.
The simulated $|S_{11}|$ and $|S_{22}|$ are less than -10 dB and -19 dB at 60 GHz which shows a good input/output matching for the designed amplifier. Figures 11 and 12 show the noise figure and stability parameters of the designed LNA respectively.

In the frequency bandwidth the stability factor \((K)\gg 1\) and stability measure \((\Delta) > 0.\) This confirms high stability of the proposed LNA.

Table I compares the performance of this LNA with those recently reported in the literature where

\[
F.O.M = \frac{\text{Gain} \times B.W}{(N.F - 1) \times P_{DC}(mW)}
\]

IV. CONCLUSION

In this letter, a 60 GHz highly stable LNA in 130nm CMOS technology have been designed. At first, the transistor’s gate width is selected for optimum noise figure and gain performances. Then, to achieve low noise figure and high stability factor the optimum length of both gate and source transmission lines are obtained. The proposed LNA achieves a high stability factor in the desired bandwidth and a gain of 14dB and a noise figure of 4dB at 60GHz.

REFERENCES


