A Low Power, Millimeter Wave Current-Reuse Cascade Amplifier in 130nm CMOS Technology

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Abstract — This paper presents a 60 GHz low noise amplifier (LNA) that adopts current reused cascade topology to reduce power consumption. By using a gate inductor a cascade connection is formed by the feed-through of the high-frequency signal through the gate-source capacitor, which results in gain-boosting. The LNA was designed in 130nm CMOS technology and simulated using ADS software. To achieve precise results, accurate models are used for microstrip transmission lines. Simulation results show the single stage gain of 12.2 dB, noise figure of 6.1 dB with the average power consumption of 8.1 mW from a 1.5V supply voltage at 60GHz.

Keywords – CMOS, Millimeter Wave, Cascode, Cascade, Resonance, CRCA

I. INTRODUCTION

Recently, interests in millimeter-wave applications such as broadband radio communication, radiometry, radio astronomy, quick downloads, imaging and car radar have been rapidly growing [1]. Historically, the design of radio front-ends and their building blocks in the 60 GHz band was based on compound semiconductors due to their very high unity gain frequencies. Nowadays, CMOS technology is expected to enable low-cost mm-wave applications such as high data-rate communication links [2]. In a receiver front end, a low noise amplifier needs to attain a large gain and low noise with the minimum possible power consumption and area. An attractive solution is a \( g_m \)-boosted common-gate LNA [3].

Several CMOS LNA designs at millimeter-wave frequencies have been reported [4]-[8]. A 60GHz low power, low voltage LNA using forward body bias, was fabricated in 90nm CMOS process was presented in [4]. The design and fabrication of a highly stable four stage cascaded LNA in the millimeter wave band in 130nm process was introduced in [5]. The stability factor of the designed LNA exceeds 3 by using a sufficient source degenerated inductor. A 60 GHz LNA in standard 130nm CMOS process was reported in [6]. [7] reported a Current-Reused Cascade Amplifier (CRCA) in 90nm CMOS process and achieved a peak gain of 12 dB and a 6.9 dB NF at 51GHz while dissipating the DC power of 7mW. The designed current-reused LNA comprises two stacked common source amplifiers with the same dc current for each stage to enhance the power gain.

[8] presented a millimeter-wave three-stage common source LNA in 130nm CMOS technology, using CPW transmission lines, which achieved a gain of 12, a NF of 8.8 dB and dissipated 36mW from a 1.5V supply.

However, most of mentioned works show high power consumption and large area (number of transmission lines).

In this paper, a 60 GHz one-stage current-reused LNA in 130-nm CMOS process is presented. This amplifier reuses the drain current to bias two transistors, feeding the signal from one stage to the other through a resonance path between the source and the gate of the common-gate MOSFET. The proposed LNA consists of only 8 microstrip lines and can be integrated into the transceiver circuit at the 60 GHz band.

II. AMPLIFIER DESIGN

A. Theory of Operation of Current-Reuse Cascade Amplifier

As the operation frequency increases it is difficult to achieve high gain using a single stage amplifier. Moreover, increasing the number of stages in a cascade connection increases the power consumption. Therefore, the approach to optimum power usage is to improve the gain of each single stage block. In order to achieve the high gain performance in millimeter wave band, the cascade configuration is widely used by LNA designers. The main drawback in cascode topology is that the common gate MOSFET does not effectively contribute to the gain. This transistor may increase the output impedance but it does not increase the gain in the amplifier because the load impedance is limited to a low value at high frequency. As a result, common gate transistor is mainly used to improve the reverse isolation. To improve the gain, the function of the common-gate transistor should be changed to that of a common source which leads to current-reuse topology. Figure 1 shows the schematic of the current-reuse amplifier where an inductive transmission line at the gate of a common-gate transistor is used. This inductive transmission line resonates with the gate-source capacitor of \( M_2 \), creating a signal path to the gate of this transistor. Hence, the source impedance of \( M_2 \) approaches to zero at the resonance frequency and \( M_2 \) operates as a
common source transistor to improve the gain of the amplifier.

![Current-Reuse Amplifier structure](image)

In Figure 1, M2 is cascaded upon M1 to reuse the bias current. The output of M1 is connected to the input of M2 through a matching circuit.

**B. Matching Elements**

IC fabrication technology is suitable for implementing the transmission lines of planar structures. As compared to coplanar waveguides (CPW), microstrip lines have higher effective inductance per unit length and more flexibility in connections. The ground plane also shields signal paths from lossy substrate. The microstrip lines are therefore good candidates for implementing the matching circuit elements.

In 0.13 µm CMOS technology, the microstrip line structure appears as in Figure 2.a, which consists of the thick top metal layer (M8) as the signal stripline and the first metal layer (M1) as the ground plane. A viable model shall include both the dielectric parameters of relative permittivity \( \varepsilon_r \), thickness H, and loss tangent (TanD), and the parameters of strip line thickness T, and metal conductivity [6].

![Microstrip line structure](image)

Microstrip line structure in Figure 2.a is different from traditional one as shown in Figure 2.b, of which the signal line is sit on top of the silicon dioxide. In ADS simulator the metal and dielectric parameters are defined in the component called MSUB (Microstrip Substrate), and the microstrip line dimensions in the component MLIN (Microstrip Line).

Modeling of the structure in Figure 2.a has been successfully put into practice in these components. Figure 3 shows the MSUB component in ADS simulator with the two adjusted parameters: The \( \varepsilon_r \) and TanD values are set to 4.8 and 0.02 to match with the practice [6].

**III. PROPOSED AMPLIFIER**

Figure 4 shows the proposed amplifier using current-reuse topology. The transistor parameters such as the gate width, length and biasing voltages are chosen for minimum noise figure and maximum gain. Both transmission lines in the gate of M2 and source of M1 are inductive and modeled by modified microstrip line model in ADS described in section II.B. In Figure 4, TL1-6 are placed for impedance matching. In order that both transistors have the same DC current, TL4 is used as an open-stub.
Figures 5 and 6 show variations of the stability factor (K) and the power gain (S_{21}) with inductance of TL_s at 60 GHz for a single common-source topology respectively. As can be seen, for small inductance values of TL_s the stability factor is less than unity and the amplifier is unstable. Therefore, L_s is selected 40pH as a tradeoff between stability and power gain.

Figure 6. Variations of power gain versus source inductance (L_s) at 60GHz.

IV. SIMULATION RESULTS

Figure 7 depicts the simulated S-parameters of the designed amplifier. This LNA achieves a maximum power gain of 12.2 dB at 60 GHz. Figure 8 displays the simulated noise figure that exhibit the minimum NF of 6 dB at 61 GHz and NF of 6.1 at 60 GHz. The total power consumption is 8.1 mW.

Figure 7. Simulated S-parameters of the proposed amplifier.

Figure 8. Simulated Noise Figure of the proposed amplifier.
The amplifier has the stability factor of 1.7 and the stability measure ($\Delta$) of 0.9 at 60GHz. Then the K-$\Delta$ condition for stability is satisfied at 60GHz. The input 1 dBm compression point of the amplifier is -18.5 dB. Using analytical calculation, the IIP3 can be estimated as -8.9 dBm which is 9.6 dB higher than actual 1-dB input-referred compression point.

Table I compares the performance of this LNA with those recently reported in the literature where

\[
FOM = \frac{\text{Gain}}{(\text{NF} - 1) \times P_{dc}(\text{mW})}
\]

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V. CONCLUSION

In this paper, a 60 GHz low power, current-reuse LNA in 130 nm CMOS technology has been designed. At first, the transistor parameters and bias are selected for optimum noise and gain performances. Then, to achieve minimum noise figure and desired gain, the optimum value for the source inductor is obtained. By connecting an inductor at the gate of the common-gate MOSFET, the role of this transistor changed to common-source one and the gain increases without increasing power consumption.

The presented LNA achieves a 12.2 dB peak $S_{21}$ gain, a 6.1 dB NF, and a -8.9 dBm IIP3 at 60 GHz while dissipating the DC power of 8.1 mW from a 1.5V supply voltage.

REFERENCES


1 Number of Transmission Lines.