Doping Concentrations Analysis on The Performance of Vertical Strained-SiGe Impact Ionization MOSFET Incorporating Dielectric Pocket (VESIMOS-DP)

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***Abstract*— The Vertical Strained SiGe Impact Ionization MOSFET incorporating Dielectric Pocket (VESIMOS-DP) has been successfully developed and analyzed in this paper. The effect of doping concentration for both Source and Drain (S/D) as well as body doping concentration to the performance of VESIMOS-DP in terms of subthreshold slope (S), threshold voltage (V_{TH}) and drain current has been observed in this paper. An inverse proportional of S and V_{TH} value was found when S/D doping concentration increased. It is notable that for S/D doping concentration above 10^{19} atoms/cm^3, there is a significant increase in S values which is not recommended as the switching speed getting higher distracting performance of the device. However, too low S/D doping concentration is not essential as it didn't show any significant improvement on the performance of the device. It is also revealed that with low body doping concentration, the device suffers tremendous Parasitic Bipolar Transistor (PBT) effect that prevents the device from switched off. Thus, optimum doping concentration is imperative to obtain superb device characteristic. Due to the DP layer, a stable V_{TH} =1.35V obtained due to the vicinity of DP layer near the drain end has reduced charge sharing between the source and drain. The slight different and consistency of VESIMOS-DP subthreshold value (S = 19 mV/dec) has given advantages for incorporating DP layer near the drain end. In many aspects, it is revealed that the incorporation of DP has enhanced the electrical performance and suppressed PBT effect of IMOS in the nanometer regime for future development of nanoelectronic device.**

Keywords- IMOS; Dielectric Pocket; VESIMOS; VESIMOS-DP; Parasitic Bipolar Effects; nano-electronics; Strained

I. INTRODUCTION

Since the 1960's the price of one bit of semiconductor memory has dropped 100 million times and the trend continues. The cost of a logic gate has undergone a similarly dramatic drop. This rapid price drop has stimulated new applications and semiconductor devices that improved the ways people carry out all human activities. The primary engine who powered the ascent of electronics is "miniaturization". By making the transistors and the interconnects smaller, more circuits can be fabricated on each silicon wafer and therefore each circuit becomes cheaper. Miniaturization has also been instrumental in the improvements in speed and power consumption.

Gordon Moore made an empirical observation in the 1960's that the number of devices on a chip doubles every 18 months or so [1]. The "Moore's Law" is a summary description of the persistent periodic increase in the degree of miniaturization. Aggressive scaling of CMOS technology into nanoscale dimensions has shown a tremendous progress in recent years demonstrated by a variety of novel device structure with an enhanced performance. As complementary metal oxide semiconductor (CMOS) scaled into the nanometer regime, the material set and device structure employed by the conventional field effect transistor (FET) are beginning to reach its physical shrinkage limits. Non-scalability of the subthreshold slope (S) and adverse short channel effects degrading the current drivability and electron mobility of a MOSFET.

An innovative device structure with appropriate device physics understanding is vitally needed for scaling the silicon MOSFET into nanometer regime. Underlying this problem is the subthreshold slope concept, which is a measure of switching abruptness in a transistor. S is fundamentally limited at 60mV/decade by the drift-diffusion based transport in current CMOS technology [2-6]. Impact ionization MOSFET (IMOS) that works on the principle of avalanche breakdown mechanism has become promising candidate to overcome this S value constraint [7]. IMOS device works on the principle of avalanche breakdown mechanism by modulating the channel length to switch between OFF and the ON states.

A very steep subthreshold slope, around 10-15 mV/decade was measured for the planar IMOS which indicate good I_{ON}/I_{OFF} ratio and low subthreshold leakage currents [8-9]. This is due to the strong dependency of Impact Ionization (II) coefficients on the electric field and the feedback inherent in the avalanche multiplication process. However, the planar IMOS exhibit severe limit which it requires high supply voltages for breakdown to occur. Such a high voltage causes damage by hot carriers to the oxide, which leads to a tremendous shift of the threshold

voltage. This instability limits the proper operation of the device and suffers from poor reliability [10-11].

Aside from the poor reliability that IMOS suffers from, it is much difficult to fabricate IMOS due to additional photolithography steps and limited by the alignment error. The gate, source and drain region are formed using separate masks which means that the gate length (L_{GATE}) and i-region length (L_I) are too difficult to be align accordingly between each other. Thus, require a lot of masking and increase the fabrication cost. In order to reduce the fabrication cost, a self-aligned n-channel IMOS was introduced [12]. The proposed structure demonstrates a self-alignment transistor that operated with a small subthreshold slope of about 7.2 mV/decade at a bias of $V_{GS} = -5.5V$ and $V_{DS} = -1.0V$ in room temperature was obtained which shows a significant improvement in term of the supply voltage when compared to the original IMOS. However, the ratio between ON and OFF current is far below the respective ratio of more than 5 orders of magnitude reported in [8].

Though the above mentioned lateral IMOS structures have significant improvement over the original IMOS [7], they still suffer from high supply voltages and damages to the oxide by hot electrons. These hot carrier effects cause abrupt shifts in the threshold and subthreshold voltages, thus resulting in poor device reliability. The lowest supply voltage reported so far is 4.8V [13]. In order to overcome those problems, vertical IMOS is developed and investigated [14-15]. The device structure is similar to the gated triangular barrier diode, which is also known as planar doped barrier FET (PDBFET). This vertical IMOS is not based on avalanche breakdown like the lateral IMOS. Instead, the holes generated by impact ionization charge the floating p-body and cause a dynamic reduction of the threshold voltage, which leads to an extremely fast rising drain current in the subthreshold region.

One of the most important advantages of the device is that it offers the mechanisms for mitigating the damages by hot electrons almost completely [16] and show the capability of working properly under high temperatures [17]. The hot carriers are spread into the bulk, not confined to the silicon-oxide interface. As a result, the device can reduce damage by hot electrons almost completely and has stable operation. Unlike planar IMOS, the vertical structure does not suffer either from V_{TH} shifts or a change in subthreshold slopes with repeated measurements. Therefore, it was observed that the vertical concept of IMOS is better than the planar IMOS in terms of hot carrier effects and device reliability. However, the device suffers from hysteresis.

This phenomenon can be explained by the parasitic bipolar transistors formed at high drain voltage. When the current originating from this bipolar transistor exceeds a certain level, the device can no longer be turned off by reducing the V_{GS}. At that time, the bipolar transistor itself delivers the electrons which provide the holes in its base current via impact ionization. Another disadvantage of the device is its low switching speed. To switch the device completely off, the floating body has to be discharged completely via the body source junction. Recently, a novel type of IMOS, called IQMOS has been reported [18]. It exploits impact ionization in a different way from the IMOS was. The IQ-FET resembles a conventional depletion-mode MOSFET with a source and drain of the same doping type, contrary to the IMOS. The cross section geometry contributes to the charge control, which results in excellent controllable and repeatable hysteresis curves, which are of great interest for memory applications.

Strain engineering has been applied as an attempt to bring the V_{DS} even further down and improve device performance. The concept of strained SiGe incorporated into the structure of vertical IMOS was introduced and investigated [19-22] as an attempt to bring down the supply voltages. Both the relaxed vertical Si IMOS and the strained SiGe vertical IMOS were studied and compared in terms of the device performance. This compressive strain developed results in high carrier mobility, high impact ionization rates and better ON-OFF current ratios, besides retaining the good subthreshold slopes shown by vertical IMOS devices. The strained SiGe vertical IMOS (Ge=20%) showed lower impact ionization coefficients than relaxed Si, but showed higher ionization rates. This was explained by alloy scattering, which reduces the number of electrons at higher energies. However, this device suffers low breakdown voltage and parasitic bipolar transistors (PBT) effect [23-25]. Hence, to obtain low threshold voltages at relatively lower supply voltage and suppressing PBT effect, dielectric pocket (DP) is incorporated into Vertical Strained-SiGe Impact Ionization MOSFET (VESIMOS).

Dielectric pocket technology being proposed in an attempt to limit dopant diffusion and reduce short channel effect and leakage current in planar CMOS [26]. It was also being introduced into the vertical MOSFET for the same reason [27]. It is revealed that the DP structure can reduce electrical bulk punch-through effects by preventing encroachment of the dopants from the extrinsic drain and reduces the charge sharing effects associated with the reverse-biased source to improve threshold voltage control [28]. The vicinity of DP in the channel region also helps to improve threshold voltage stability, electron velocity of the device and suppressed the Parasitic Bipolar Transistor (PBT) effect [29-31]. Hence, improve the functionality of the device. With the vicinity of DP, a much greater and beneficial reduction of I_{OFF} arises thanks to the suppression of both drain induced barrier lowering and tunnelling.

In this paper, the effect of doping concentration for both Source and Drain (S/D) as well as body doping concentration to the performance of Vertical Strained-Sige Impact Ionization MOSFET incorporating Dielectric Pocket (VESIMOS-DP) in terms of subthreshold slope, threshold voltage and drain current has been observed. In short-channel devices, doping concentration can impact the threshold voltage roll off, subthreshold slope degradation and the drain-induced barrier lowering (DIBL) effect [32-35]. Hence, doping concentration needs to be in optimum value in order to have an appreciable effect on the improvement of SCEs.

II. DEVICE STRUCTURE AND CONCEPT

Fig. 1 depicts the detailed cross-sections of the Vertical Strained-SiGe Impact Ionization MOSFET with dielectric pocket simulated using Sentaurus Tool package [36] for performance analysis. This structure comprises a source and a drain region with n^+ doping, an intrinsic channel containing a highly doped delta p^+ (δp^+) layer and two sided gates. The high doping of the delta layer which creates a large potential barrier, makes it possible to achieve high electric fields in the intrinsic zone near the drain without applying a very high drain–source voltage [14]. Careful selection of the delta layer thickness is recommended as to have good sub-threshold slopes. Hence, an optimum value of delta layer thickness and doping was chosen to get desired sub-threshold slopes.

The intrinsic-Si (i-Si) regions reduce the lateral electric field near the source and the drain [20]. Therefore, an optimum thickness for i-Si region has been chosen, so that they could effectively reduce the lateral electric fields. Due to the presence of i-Si regions between highly doped S/D regions, the impurity scattering is also reduced. The strained layer thickness was 20nm with Ge=30%. The DP layer thickness was also 20nm. Nonetheless, the DP layer thickness was varied to examine its effects towards device performance. The DP layer was also sandwiched with intrinsic Silicon caps with 5nm thickness. This Si-cap acts the same function as i-Si to improve the stability of the overall device. The doping concentration in the silicon S/D region is assumed to be very high with a peak value of $2.08x10^{18}/cm^3$ for negligible silicon resistance near the channel. The source and drain are n-doped with Antimony and Phosphorus respectively. However, the S/D doping concentrations is being varied from $2.08x10^{16}$ to $2.08x10^{20}$ atoms/cm^3 to know its effect towards device performance.

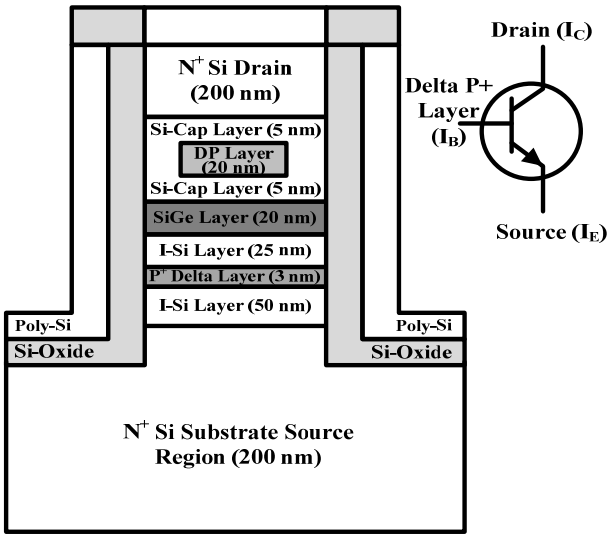

Figure 1. VESIMOS-DP device structure with respective layer thickness of source, drain, δp^+, i-Si, SiGe, Si-cap and DP.

The body region is doped with boron concentration of $4x10^{19}/cm^3$ known as δp^+ layer. The high doping of δp^+ layer makes it possible to achieve high electric field which creates a large potential barrier. However, the body doping of the highly doped δp^+ layer will be vary to know its effect towards device performance. The δp^+ layer is stacked between two intrinsic zones as active region between n^+ source and drain regions. This intrinsic region known as i-Si regions helps to reduce the lateral electric field near the source and drain. The presence of i-Si regions also reduces the impurity scattering between the highly doped S/D regions. VESIMOS-DP shows three distinguish operating modes; conventional MOSFET, Impact Ionization and Bipolar (BJT) mode. In conventional MOSFET mode, low V_{DS} and insufficient electric field limit the II rate. The barrier is lowered by V_{GS} and an electron channel is formed below the gate between i-Si and δp^+ region.

As the V_{DS} rise, the electric field in the drain side intrinsic region increased until the impact ionization rate occurs in the drain side intrinsic zone. The device is now in the II mode. The potential barrier is lowered by V_{GS}, thus allows the electron from the source travel into the drain region. In this II mode, a significant lower subthreshold swing value is obtained due to the extremely fast rising current in the subthreshold region. This current amplification is not caused by the impact ionization rate like in lateral IMOS. Instead, the holes generated by the II accumulated in the δp^+ layer region charged the body of the transistor and causing a dynamic reduction of threshold voltage during switch ON operation [16]. Hence, a very good subthreshold and I_{ON}/I_{OFF} ratio is obtained in this mode. The impact ionization rate depends on the electric field in the drain-side intrinsic region. Increasing the V_{DS} will increase the II rate exponentially. This leads to the rising hole current in the δp^+ layer region.

At a point when the δp^+ layer region cannot contain with the surge of holes currents, the gate loses its control over the drain current. The third operating mode is initialized, which is BJT mode. As the drain source current (I_{DS}) increase, the holes generated by II in the δp^+ region also increases which act as a base current. In this mode, the n^+ drain region act as a collector, the n^+ source region as an emitter and δp^+ layer as a base [23] as depicted in Fig. 1. A small current entering the base is amplified to produce a large collector and emitter current. When there is a positive potential difference measured from the emitter to its base as well as from the base to the collector, the transistor becomes active. In this ON state, current flows between the collector and emitter of the transistor same like the bipolar junction transistor operation as depicted in Fig. 2.

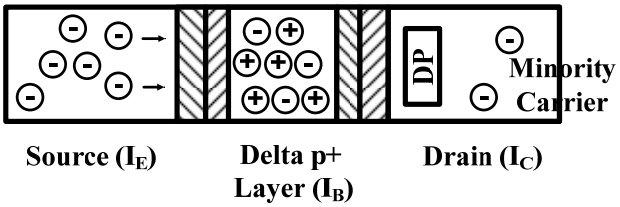

Figure 2. Parasitic Bipolar Transistor (PBT) effect principle of VESIMOS-DP device in Bipolar (BJT) mode.

Most of the current is carried by electrons moving from emitter to collector as a minority carriers in the P-type base region. Although even lower S value is obtained, a significant hysteresis is observed in the input characteristic at this operating mode [16]. The S value of the input characteristic keeps changing and the device experiencing V_{TH} roll-off in this operating mode due to the PBT effect. When the V_{DS} in the δp^+ layer region exceeds a certain level, the device can no longer be switched OFF. This is called Parasitic Bipolar Transistor (PBT) effect. To counteract this effect, V_{DS} has to be reduced below the level necessary for II to occur or apply a negative V_{GS} in order to switch OFF the device again [17]. The introduction of DP into the device structure also helps to eliminate the PBT effect.

III. Device Performance Analysis

VESIMOS-DP device mechanism is different with a lateral IMOS which use impact ionization rate as a current amplification. Instead, a positive gate voltage reduces δp^+ triangular shaped barrier and allows electron to flow from source to drain. With rising drain source voltage, the electric field at the drain side intrinsic zone becomes high enough to cause impact ionization to occur in this region. The holes generated by the II accumulated in the δp^+ layer region charged the body of the transistor and causing a dynamic reduction of V_{TH} that let the electrons to accelerated towards the drain region. The transfer characteristic is examined by biasing the drain voltage and ramping the gate voltage at defined bias steps. Fig. 3 shows the comparison of transfer characteristic, I_{DS}-V_{GS} of VESIMOS-DP with different DP size ranging from 20nm to 80nm.

Fig. 3 revealed that VESIMOS–DP works well for low power supply voltage (V_{DS}=1.75V), which has overcome problem faced by the conventional IMOS devices [7-13]. The transfer characteristic of VESIMOS-DP shows stable and consistent S and V_{TH} across different DP size from 20 to 80nm of about 19 mV/decade and 1.35V respectively. There is slightly higher threshold voltage obtained for 80nm DP as it requires more energy to pass through a higher potential barrier compared to the others. The reason for the stability of S and V_{TH} is due to the carrier transport of VESIMOS-DP, which is not confined to the oxide-silicon interface like in the lateral IMOS where hot carriers are injected into the oxide and cause traps that lead to the shift of V_{TH}.

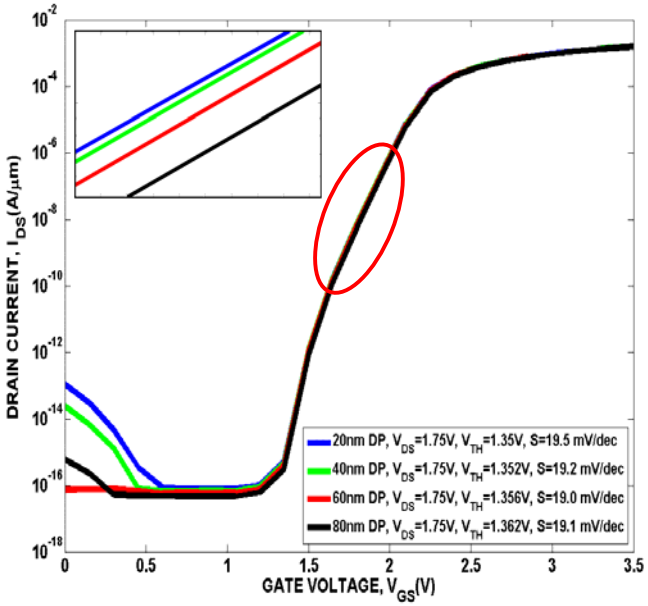

Figure 3. Transfer Characteristics, I_{DS}-V_{GS} of VESIMOS-DP for $Si_{0.7}Ge_{0.3}$, S/D doping = $2.0x10^{18}/cm^3$, $N_A = 4.0x10^{19}/cm^3$ V_{DS}=1.75V.

In the vertical IMOS, the channel spreads out into the bulk [23] where the impact ionization takes place. The main carrier transport between the delta layer and drain takes place in the bulk region. This is obviously the main reason for the stability of the device. The presence of DP layer also has reduced charge sharing between source and drain that helps to improve reliability of the device. This analysis can be summarized as in Table 1, which shows the comparison of threshold voltage and subthreshold voltage obtained for VESIMOS–DP device with different DP size. From table 1, it can be observed that the DP with 60nm size has superb performance as it has lowest subthreshold value (S=19.0 mV/decade) and lower threshold voltage (V_{TH} =1.356V) when compared to others. Taking that into the consideration, VESIMOS–DP with 60nm DP were being used to analyze the effect of doping concentration on the performance of VESIMOS-DP device throughout the paper.

TABLE I. VESIMOS–DP V_{TH} AND S AT DIFFERENT MODES OF OPERATION

DP Size (nm)	**20nm**	**40nm**	**60nm**	**80nm**
V_{TH} (V)	1.35	1.352	1.356	1.362
S (mV/decade)	19.5	19.2	19.0	19.1

Fig. 4 demonstrates the transfer characteristic of VESIMOS-DP at different S/D doping concentrations. The S/D doping concentrations is being varied from $2.08x10^{16}$ to $2.08x10^{20}/cm^3$ to know its effect on the device performance.

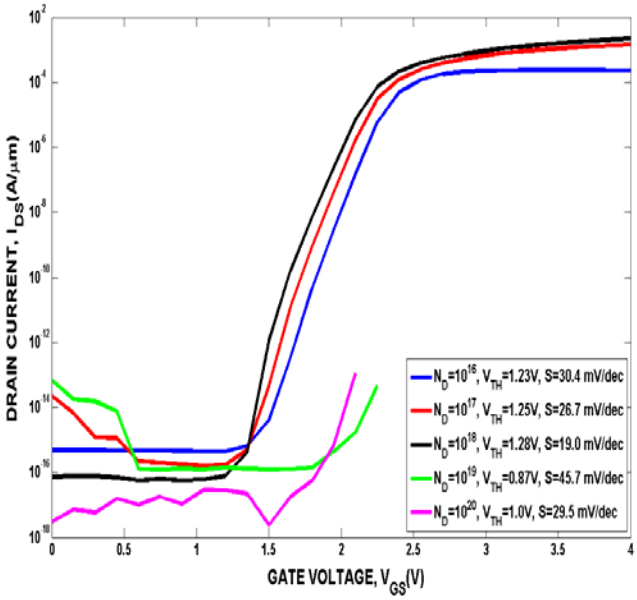

Figure 4. Transfer Characteristics, I_{DS}-V_{GS} of VESIMOS-DP for $Si_{0.7}Ge_{0.3}$, S/D doping = $2.0x10^{18}/cm^3$, $N_A = 4.0x10^{19}/cm^3$ V_{DS}=1.75V at different S/D doping concentration.

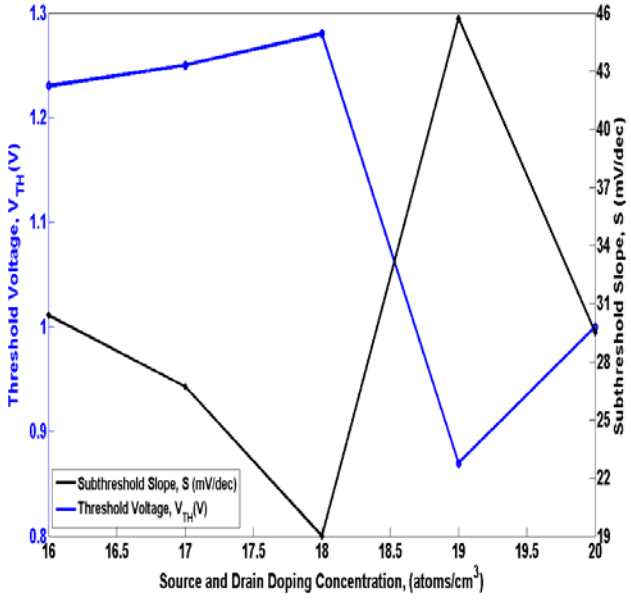

Figure 5. VESIMOS-DP Threshold Voltage and Subthreshold slope variation at different S/D doping concentration.

The S/D doping concentrations are necessary to obtain superior device characteristic as the device concept was based on impact ionization mechanism which requires high electric fields. Both the drift current and electric field depends on the doping concentration in order to achieve the desired device characteristic. Fig. 4 shows that the V_{TH} increase as the S/D doping concentration increases. Optimum S/D doping concentration is essential to obtain good device characteristic. As shown in the graph, the V_{TH} keeps increasing until a certain point ($N_D=10^{18}$) then drop beyond that concentration. However, it affects the S value which is unfavorable as it start to increase above the concentration. This will affect the switching speed of the device which disrupt the good features found in the IMOS device. The high S/D doping concentration is essential for negligible silicon resistance near the channel. However, too high S/D doping concentration is not recommended as it affects the performance of the device (S=29.5mV/decade) as shown in the graph above.

Fig. 5 shows the variation of threshold voltage and subthreshold slope at different S/D doping concentration. The high S value in high S/D doping concentration is due to the fact that there are no potential difference between n^+ S/D region and p^+ delta layer region where the electron travel from low concentration region to the high concentration region. Thus affect the mobility of the electron to switch ON the device. The high S/D doping concentration causing the electron to keep pushing into the δp^+ layer without allowing the electron from the source to penetrate through the δp^+ layer region to ON the device.

Fig. 5 revealed that there are significant drop (from S=30mv/dec to S=19mv/dec) in subthreshold slope while threshold voltage is increase as the S/D concentration increases. It is notable that for S/D doping concentration above 10^{19}, there is a significant increase in S values which is not recommended as the switching speed getting higher distracting performance of the device. However, too low doping concentration is not essential as it didn't show any significant improvement in the performance of the device. Thus, optimum S/D doping concentration ($N_D=2.08x10^{18}/cm^3$) are imperative to obtain superb device characteristic. At off-state operation mode, drain leakage current, I_{OFF} is independent to the gate voltage, but increases with the increasing drain voltage as depicted in Fig. 4.

A very low off-state leakage current, I_{OFF} = $7.3x10^{-17}$ A/μm and good drive current, I_{ON} = $1.5x10^{-10}$ A/μm taken at V_{DS} = 1.75 V obtained for optimum S/D doping ($N_D=2.08x10^{18}/cm^3$) VESIMOS-DP device. Hence, the device has good switching characteristics because of high I_{ON}/I_{OFF} ratio which approximately 10^7. This is due to the triangular barrier concept which effectively keeps the leakage current low. However, for low S/D doping ($<N_D=2.08x10^{18}/cm^3$), the off-state leakage current increase which affect the performance of the device. Although very low off-state leakage current, I_{OFF} = $3x10^{-18}$ A/μm and good drive current, I_{ON} = $5x10^{-17}$ A/μm taken at V_{DS} = 1.75 V were observed for very high S/D doping ($>N_D=2.08x10^{18}/cm^3$), the device doesn't operate at high V_{DS} ($>V_{DS}$ = 2V) which is not recommended.

This can be summarized in Table 1, which shows the comparison of threshold voltage, subthreshold slope and I_{ON}/I_{OFF} ratio obtained for VESIMOS-DP device at different S/D doping concentration

TABLE II. VESIMOS-DP V_{TH} AND S AT DIFFERENT S/D DOPING CONCENTRATION

S/D doping concentration (atoms/cm3)	**<10^{18}**	**10^{18}**	**>10^{18}**
V_{TH} (V)	1.23	1.28	0.87
S (mV/ decade)	30.4	19.0	45.7
I_{ON}/I_{OFF}	10^3	10^7	10^1

The Body doping concentration was also varied in this paper to examine its effect on the device characteristics of VESIMOS–DP device. VESIMOS-DP with 60nm DP size were used to simulate the effect of body doping concentration towards device performance. The body doping concentration in δp^+ region is being varied from $4x10^{10}$ to $4x10^{23}/cm^3$. In short-channel devices, body doping can impact the threshold voltage roll off, subthreshold slope degradation and the drain-induced barrier lowering (DIBL) effect [32]. When body doping level is high, carrier mobility in the channel can be strongly degraded by the dopants. Heavy body doping also causes strong band-to-band tunneling from body to the drain that can be a source of leakage current [33]. Body doping also gives rise to a discrete dopant fluctuation effect, which contributes to additional threshold voltage variation [34]. Increase in body doping also gives rise to a higher electric field. Hence, body doping needs to be in optimum value in order to have an appreciable effect on the improvement of SCEs. Fig. 6 depicted transfer characteristic of VESIMOS–DP at different body doping concentration.

Fig. 6 shows that the V_{TH} increase as the body doping concentration increases. High body doping is essential to form highly δp^+ potential barrier separating two n^+ doped source and drain. The supply of drain voltage provides sufficient energy for the electrons to cross the δp^+ and DP potential barrier forming ON current. As the V_{DS} increases, the electric field in the drain side intrinsic region increased until the impact ionization rate occurs in the drain side intrinsic zone that allows electron flow from source to drain. This justified the increase in threshold voltage at high body doping concentration as it requires more energy to overcome both highly δp^+ and DP potential barrier.

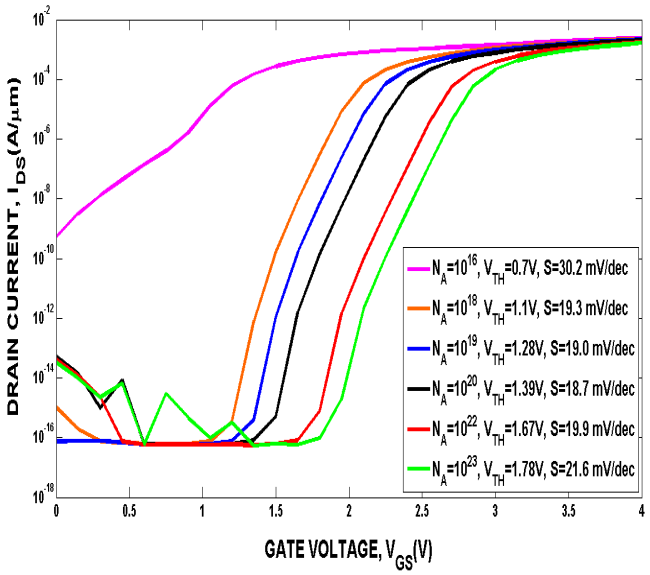

Figure 6. Transfer Characteristics, I_{DS}-V_{GS} of VESIMOS-DP for $Si_{0.7}Ge_{0.3}$, S/D doping = $2.0x10^{18}/cm^3$, N_A = $4.0x10^{19}/cm^3$ V_{DS}=1.75V at different body doping concentration..

At off-state operation mode, drain leakage current, I_{OFF} is independent to the gate voltage, but increases with the increasing drain voltage as depicted in Fig. 4. A very low off-state leakage current, I_{OFF} = $7.3x10^{-17}$ A/μm and good drive current, I_{ON} = $1.5x10^{-10}$ A/μm taken at V_{DS} = 1.75 V obtained for high doping (>N_A=$4.0x10^{18}/cm^3$) VESIMOS-DP device. Hence, the device have good switching characteristics because of high I_{ON}/I_{OFF} ratio which approximately 10^{-6}. This is due to the triangular barrier concept which effectively keeps the leakage current low. Fig. 7 shows the variation of threshold voltage and subthreshold slope at different body doping concentration.

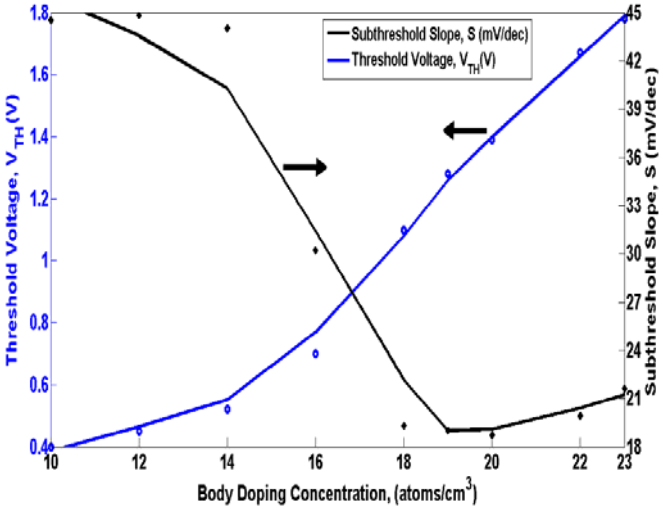

Figure 7. VESIMOS-DP Threshold Voltage and Subthreshold slope variation at different body doping concentration..

Fig. 7 revealed that there are significant drop (from S=40mv/dec to S=19mv/dec) in subthreshold slope while threshold voltage is increase as the body doping concentration increases. It is notable that for body doping concentration above 10^{20}, the S values keep increasing which is not recommended as the switching speed getting higher distracting performance of the device. The high S value in low body doping concentration is due to the fact that the δp^+ region is not properly formed to build the potential barrier between the n^+ source and drain. The holes are not confined in the δp^+ layer which causing the npn channel region not properly created. Hence, the device behaves like conventional CMOS. This justified the high S value and low V_{TH} as there is no high potential barrier to get through. Hence, high body doping concentrations are imperative for obtaining better device characteristics and ensure the device works in II mode. In addition, the output characteristic was also highlighted a very good drain current at different gate voltage with the increasing of drain voltage for VESIMOS–DP with high body doping concentration as shown in Fig. 8.

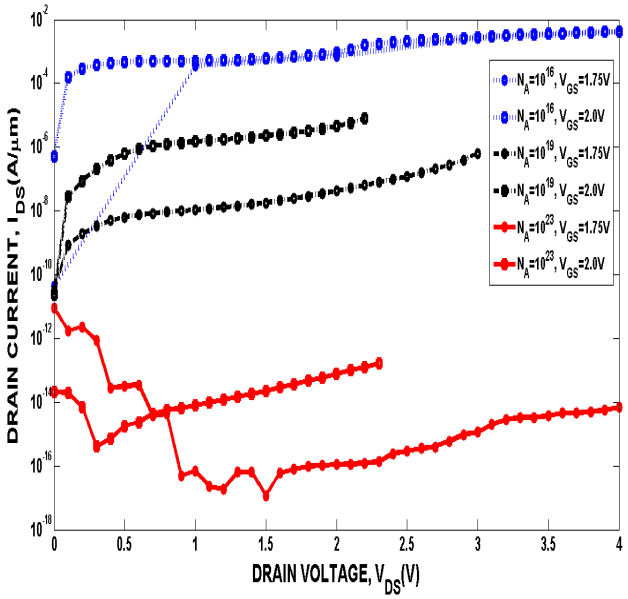

Figure 8. Output characteristics of VESIMOS-DP for $Si_{0.7}Ge_{0.3}$, S/D doping =$2.0x10^{18}/cm^3$, V_{GS}=1.75V and V_{GS}=2.0V at different body doping concentration.

It can be seen from Fig. 8 that initially the drain current rises sharply and then increases gradually before going into breakdown for VESIMOS-DP with $N_A=4.0x10^{19}/cm^3$. The sharp rise in drain current can be attributed to the presence of Ge. Germanium has high and symmetric impact ionization rates ($\alpha_N \approx \alpha_P$), which ensures that the transition from OFF state to the ON state is abrupt [19]. For VESIMOS-DP < $N_A=4.0x10^{19}/cm^3$, the device instead of going to breakdown state, it undergoes bipolar mode. In bipolar mode, the current amplification mechanism contributes to the lower subthreshold slope but with a certain hysteresis due to the PBT effect. PBT effect prevents the device from being able to switch off and the device will never undergoes breakdown state. However, a very high (>$N_A=4.0x10^{23}/cm^3$) body doping is not recommended as it shows poor drive current and suffers PBT effect at high gate voltage (V_{GS}>2.0V). Hence, optimum body doping concentrations ($N_A=4.0x10^{19}/cm^3$) are imperative for obtaining better device characteristics and ensure the device works in II mode.

IV. Conclusion

The advantages of incorporating dielectric pocket (DP) that leads to the improvement of switching speed to the Vertical Strained-SiGe Impact Ionization MOSFET device has been investigated and explained. The dependency of the S/D and body doping concentration on the device performance is shown using Sentaurus TCAD tools. Due to the DP layer, a stable V_{TH} =1.35V obtained due to the vicinity of DP layer near the drain end has reduced charge sharing between the source and drain. The slight different and consistency of VESIMOS-DP subthreshold value (S = 19 mV/dec) has given advantages for incorporating DP layer near the drain end. There is a significant drop (from S=30mv/dec to S=19mv/dec) in subthreshold slope while threshold voltage is increase as the S/D concentration increases. It is notable that for S/D and body doping concentration above 10^{19}, there is a significant increase in S values which is not recommended as the switching speed getting higher distracting performance of the device. However, too low doping concentration is not essential as it didn't show any significant improvement in the performance of the device. Thus, optimum S/D doping concentration is imperative to obtain superb device characteristic and ensure the device works in II mode.

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