In-Depth Design and Simulation Analysis of Vertical Strained Impact Ionization MOSFET (VESIMOS)

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***Abstract*—The Vertical Strained Silicon Germanium (SiGe) Impact Ionization MOSFET (VESIMOS) has been successfully design and analyzed in this paper. VESIMOS device integrates vertical structure concept of Impact Ionization MOSFET (IMOS) and strained technology. The transfer characteristics of VESIMOS revealed an inverse proportionality between supply voltage, V_D and sub-threshold, S due to lower breakdown strength of Germanium (Ge) content. The S=10mV/dec was successfully obtained at threshold voltage, V_T=0.9V, with V_D=1.75V. This V_T is found to be 40% lower than V_T for conventional Si-vertical IMOS. The output characteristics goes into saturation for V_D more than 2.5V, attributed to the presence of Ge that has high and symmetric impact ionization rates. Electron mobility was improved by 40% compared to conventional Si-vertical IMOS. The increase in strain layer thickness, T_{SiGe}, resulted in an increase of V_T and lowered the mobility due to the strain relaxation in the SiGe layer. For high source-drain doping concentration, S/D=2x10^{18}/cm^3, the V_T dropped to 0.88V, with V_D of 1.75V due to high electric field effect in the channel, which is found to be contrary to the doping effects of conventional MOSFET. In every aspect, VESIMOS is projected to be premier candidate for future nanoelectronics device as to prolonged the scaling of conventional MOSFET into nano-regime.**

Keywords- Impact ionization; MOSFET; IMOS; nanoelectronics; doping effects; SiGe; Strain; Vertical MOSFET; Nanodevice

I. INTRODUCTION

For decades, silicon has been the heart of semiconductor industry which has revolutionized the world since the invention of silicon transistors by William Shockley in 1950's. It can be attributed to the concept of transistor scaling or miniaturization. Due to the realization of Moore's law [1], today, the miniaturization of silicon devices have provided a path towards denser, faster integration and better in performance with every new device that has been invented since its inception. However, Continuous scaling of MOSFETs has leads inexorably toward fundamental physical limits. A severe difficulty is the limitation of the sub-threshold slope *S* [which is defined as *dVG/d*(log *ID*)] of a MOSFET. It is governed by kT/q and has a theoretical limit of 60 mV/dec at room temperature [2]. Accordingly, high sub-threshold slopes, reduced carrier mobility and increased leakage currents which inevitably leads to high power consumption and heating questioning the reliability of smaller devices [3-5].

Lateral Impact Ionization MOSFET (IMOS) which utilized drift mechanisms of carriers rather than diffusion, is one such attempt to produce better performing devices at a nano-scale level [6-9]. IMOS works on the principle of avalanche breakdown mechanism of p-i-n diodes, induced by impact ionization. The carrier transport mechanism in this device is due to drift, rather than diffusion mechanism. This mechanism provides excellent sub-threshold slopes of less than 10-20mV/decade [10]. Nevertheless, as IMOS works on the concept of impact ionization, it requires high operating voltages which results in hot carrier degradation effects such as shifts in threshold voltage and sub-threshold slopes [11-13]. This leads to a poor reliability of the planar IMOS device.

Therefore, vertical IMOS, which is a planar-doped barrier MOSFET with a floating body, has been introduced and investigated [14-18]. The device is capable to reduce supply voltage, mitigating the hot electrons damages almost completely [14-16] and shows capability of working properly under high temperatures [17].This vertical IMOS is not based on avalanche breakdown like the lateral IMOS. Instead, the holes generated by impact ionization charge the floating p-body and cause a dynamic reduction of the threshold voltage, which leads to an extremely fast rising drain current in the sub-threshold region. To achieve desired device characteristics, relatively high supply voltages are to be provided and hence, high threshold voltages. To reduce the supply voltages, vertical IMOS with a strained SiGe layer was introduced and investigated [19-22]. A thin strained SiGe layer was placed in the channel region towards the drain-side intrinsic region of the vertical IMOS. This compressive strain developed results in high carrier mobility, high II rates and better ON-OFF current ratios, besides retaining the good sub-threshold slopes shown by vertical IMOS devices.

The concept of vertical IMOS integrated with the strained SiGe was developed by Dinh T.V. et al., (2009) [20] to bring down the device operating voltage. Although the work done was successful in attaining its objective, it did not provide an in-depth analysis on the device performance, based on strain variation. In this research study, a detailed explanation on various parameters that affect the device

performance are analyzed and discussed. This paper present a further study on the correlation between supply voltage, sub-threshold, leakage current and saturation current based on device transfer characteristics and output characteristics on Vertical Strained-SiGe Impact Ionization MOSFET (VESIMOS). Enhancement of electron mobility and strain composition effects towards threshold voltage is also studied. Finally, the effect of strain layer thickness, T_{SiGe} and doping concentration to enhance performance of VESIMOS as a potential candidate for future nanoelectronics device was also revealed.

II. Device Simulation And Structure

Fig. 1 shows the detailed cross-sections of the device structure which simulated for performance analysis of the Vertical strained-SiGe Impact Ionization MOSFET (VESIMOS) using Silvaco's package [23]. The VESIMOS device was realized with the help of simulation tools. Any electronic device, before being manufactured would be simulated first, in order to study its real-time behavior. Simulation is developing a computer-based model of a real-world system. Developing a simulation model is essential to gain a deeper understanding of the real system, under various criteria. It would also save the manufacturing industry from huge material and economic losses. Therefore, handful numbers of simulation software have been developed to simulate the process flow of the semiconductor devices and also to analyze their behavior through device simulations.

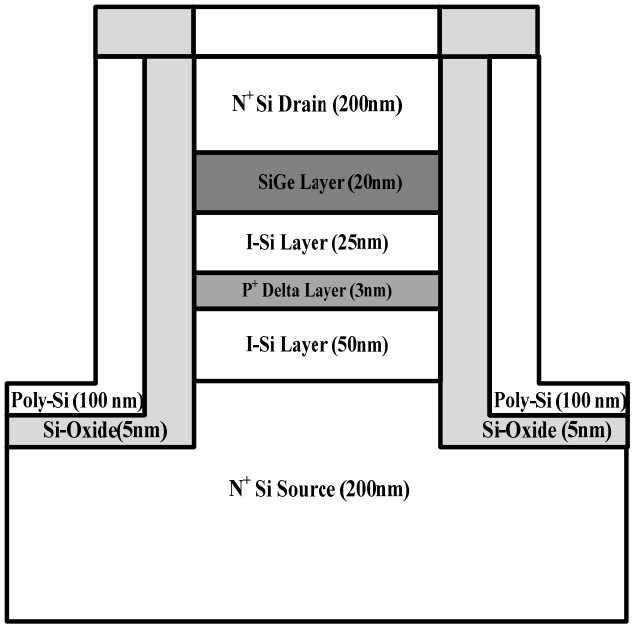

Figure 1. VESIMOS device structure with dimensions, d=0.8µm, L=0.5µm, respective layer thickness of source, drain, δp^+, i-Si, SiGe and Ge=30%.

The device structure comprises of source and drain region with n+ doping, an intrinsic channel containing a highly doped dp+ layer and two sided gates. The high doping of the delta layer, which creates a large potential barrier, makes it possible to achieve high electric fields in the intrinsic zone near the drain without applying a very high drain–source voltage, V_{DS} [20]. Careful selection of delta layer thickness is recommended as to have good sub-threshold slopes. Hence, an optimum value of delta layer thickness and doping was chosen to get desired sub-threshold slopes. The intrinsic-Si, i-Si regions reduce the lateral electric field near source and the drain [24]. Therefore, an optimum thickness for i-Si region has been chosen, so that they could effectively reduce the lateral electric fields. Due to the presence of i-Si regions between highly doped S/D regions, the impurity scattering is also reduced. The strained layer thickness was 20nm. However, the strained layer thickness was varied to examine the device performance. The increase in strained layer thickness is related to the strain relaxation. Hence, varying this parameter is essential to understand the behavior of the device under strain.

The Ge mole fraction is related to the amount of strain in the SiGe layer. The Ge mole fraction used was 30%, initially. Later, the mole fraction was varied from 10% to a maximum mole fraction of 50%. The lower the mole fraction, the lower is the strain. Hence, by varying the amount of strain, the device performance was analyzed. The Source was n-doped with Antimony with a doping concentration of $2.08x10^{18}$ /cm^3. The Drain was also n-doped with Phosphorus with a doping concentration of $2.08x10^{18}$ /cm^3. The high doped S/D doping was chosen, as the device concept was based on impact ionization. VESIMOS is an impact ionization device with drift current mechanism, which requires high electric fields. Both the drift current and the electric fields depend on the doping concentrations. Hence, high doping concentrations are imperative for obtaining better device characteristics.

The electrical characteristics of devices were done by solving Poisson's equation and continuity equation numerically and self-consistently within explicitly defined meshes of the devices [23]. The electrical potential energy and electronic band structures can be computed by using Poisson's equation. Continuity equations for electrons and holes are then used to calculate the current densities of electrons and holes. Boltzmann transport framework is used in solving these two equations. The relationship between the current density of electrons/holes and carrier concentration as well as quasi-Fermi potential is exhibited during this self-consistent process. The drift–diffusion (DD) transport model with the Boltzmann carrier transport framework was used, as it is able to predict I–V characteristics of DG-MOSFET [25]. Even for nanoscale size >10 nm, Granzneretal. [26] have shown that for DG-MOSFET's current characteristics, the DD and Monte-Carlo simulation results produced excellent agreement, while Ren and Lundstorm [27] and Rhew and Lundstorm [28] have revealed that the DD model can predict I–V characteristics of short-channel MOS devices more realistically than the energy-balance (EB) model. The

Selberherr's [29] impact ionization model was employed, which is a local impact ionization model. Selberherr's model is recommended for most cases of device simulation.

III. Results And Discussion

Fig. 2 shows the SIMS profile, showing the doping concentrations in the drain, substrate and the intrinsic regions, respectively. From figure 4.2, it can be seen that the thickness of the SiGe layer is 20nm and the Ge content is 30%. The delta layer thickness is 3nm and the intrinsic-Si layers are 50nm thick. The antimony doping at the source region is shown as $2.0x10^{18}$/cm3, the Phosphorus doping at the drain side is $2.0x10^{18}$ /cm3, the boron doping in the delta layer is $4.0x10^{20}$ /cm3 and the intrinsic-Si layer doping is approximately $1.0x10^{14}$ /cm3.

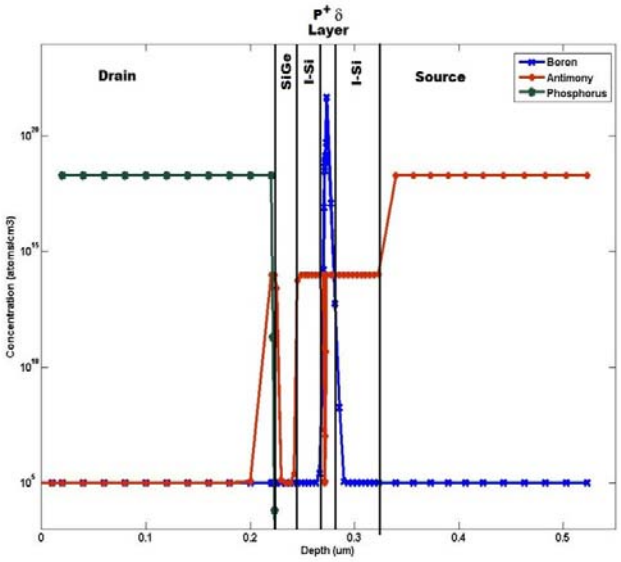

Figure 2. SIMS profile showing the doping concentration in different regions of the VESIMOS-DP structure.

VESIMOS device works in three different modes: conventional MOSFET, Impact Ionization (II) and Bipolar (BJT) mode. The transfer characteristic is examined by biasing the drain voltage, V_D and ramping the gate voltage, V_G at defined bias steps. Fig. 3 shows the I_D-V_G characteristics of the VESIMOS.

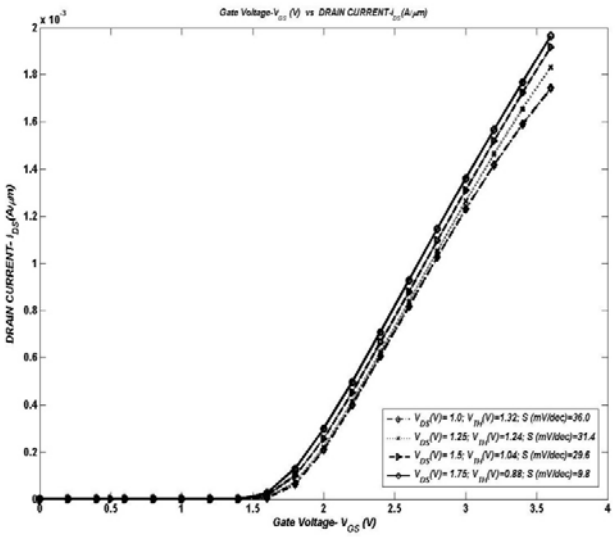

Figure 3. Current-Voltage characteristic of VESIMOS for $Si_{0.7}Ge_{0.3}$, S/D doping = $2.0x10^{18}/cm^3$.

The combination of Gummel and Newton numerical method was employed for a better initial guess in solving quantities for obtaining a convergence of the device structure. By using a linear extrapolation of transconductance gm (VGS) to zero [30] a 0.9 V threshold voltage V_T was obtained with a supply voltage, V_{DS} of 1.75V. The threshold voltage, V_T obtained is found to be 40% lower than V_T for Si-vertical IMOS [14].

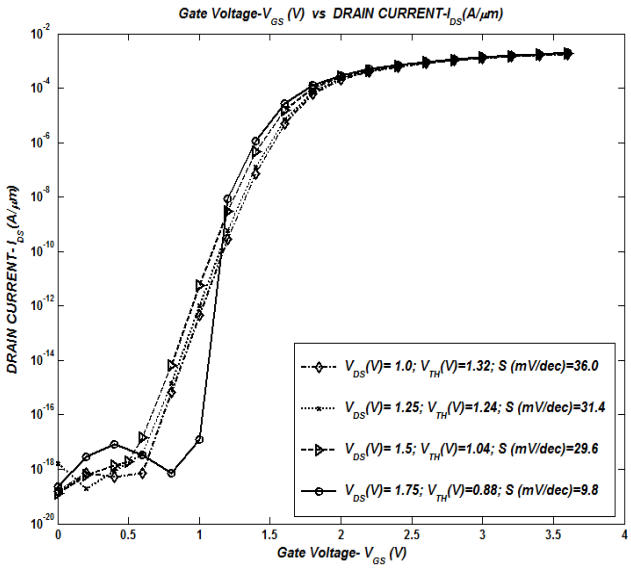

Figure 4. Transfer Characteristics of VESIMOS for $Si_{0.7}Ge_{0.3}$, S/D doping = $2.0x10^{18}/cm^3$.

Fig. 4 shows Transfer Characteristics of the VESIMOS device. It shows an inverse proportionality between the supply voltage, V_D and the sub-threshold voltage, S. This is due to the electrons having enough energy to cross the potential barrier only at high supply voltage, which is V_D=1.75V. However, beyond this value, the device undergoes breakdown, due to lower breakdown strength of Ge. Hence, it can be concluded that VESIMOS works well for lower supply voltage, which has overcome the problem faced by conventional IMOS devices [14-16]. As we know, sub-threshold voltage is in direct proportion to the leakage currents. Hence, a lower sub-threshold voltage ensures low leakage currents. For VESIMOS, a good sub-threshold voltage, S=10mV/decade was obtained. This sub-threshold voltage obtained, is much lower than the conventional MOSFET limit due to the impact ionization mechanism of VESIMOS device.

In the off-state operation mode, the transistors show a drain leakage current, I_{OFF} which is independent of the gate voltage, but increases with increasing drain voltage as depicted in Fig. 4. A very low off-state leakage current, I_{OFF} = 1 x 10^{-19} A/μm and good drive current, I_{ON} = 1 x 10^{-8} A/μm taken at V_{DS} = 1.75 V was explicitly shown. Hence, The I_{ON}/I_{OFF} ratio observed is approximately 10^{12}

TABLE I. VESIMOS V_{TH} AND S AT DIFFERENT MODES OF OPERATION

Mode	V_{DS} (V)	V_{TH}(V)	S (mV/decade)
Conventional	≤1.25	1.24	31
Impact Ionization	>1.25	0.88	9.8
Bipolar	>1.80	-	-

Table 1 shows the threshold voltage and sub-threshold voltage in various modes of operation. It shows that for V_{DS} >1.80V, the device, instead of going to the bipolar mode, as in Si vertical I-MOS device, it undergoes breakdown. This was one of the limitations observed with VESIMOS device. The low breakdown voltages of this device can be attributed to the low bandgap of the Ge compared to other semiconductor materials [31]. It is also inherent properties of Germanium (Ge), that has a breakdown strength two times lower than the Si. However, in planar doped barrier FET (PDBFET) with impact ionization devices, it was observed that for V_{DS} >1.5V, the device undergoes avalanche breakdown [32]. Based on this comparison, it can be seen that the strained SiGe vertical IMOS has a higher breakdown voltage.

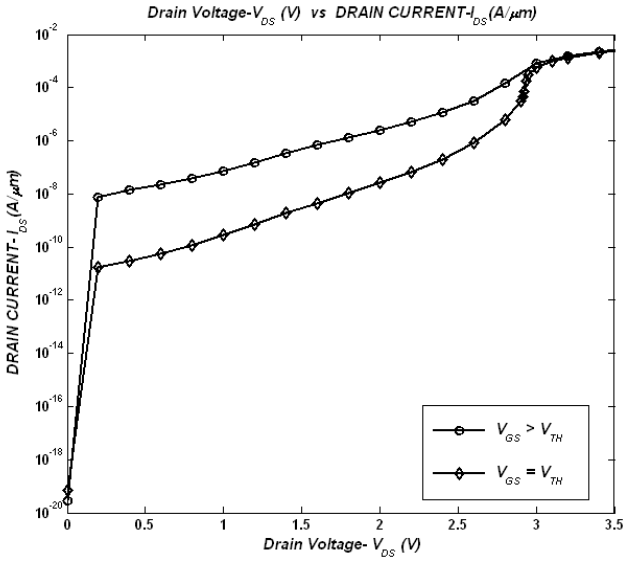

Figure 5. Transfer Output characteristics of VESIMOS device.

Fig. 5 shows the output characteristics of VESIMOS. It can be seen that the drain current rises sharply initially, and then increases gradually, before going into saturation for V_{DS} > 2.5V. The sharp rise in drain current can be attributed to the presence of Ge. Germanium has high and symmetric impact ionization rates ($\alpha_N \approx \alpha_P$), which ensures that the transition from OFF state to the ON state is abrupt [6]. Moreover, the Planar IMOS devices never go into saturation. Hence the saturation of VESIMOS, unlike planar IMOS makes it useful for digital applications in reducing the inverter delay and contributes to the gain in analog applications. This can be one of the advantages of VESIMOS over planar IMOS. The threshold voltages for various drain voltages were plotted as shown in Fig. 6.

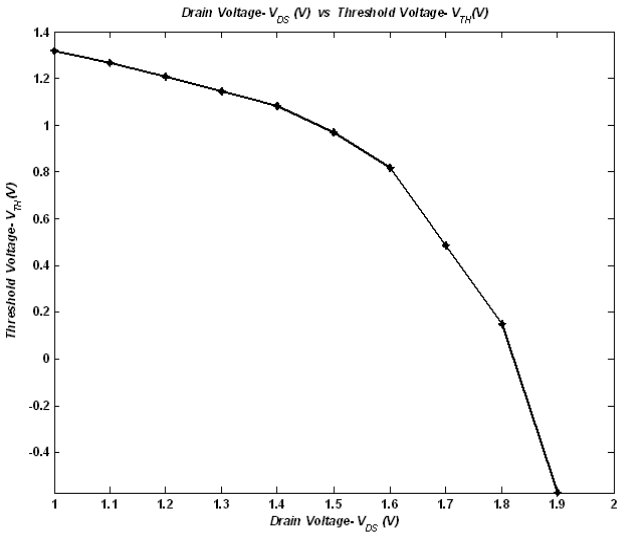

Figure 6. VESIMOS Drain voltage (V_{DS}) vs. Threshold.

The V_{DS} -V_{TH} graph shows the relationship between threshold voltage and the drain voltage. It can be observed that the V_{TH} decreases gradually with increasing of V_{DS}. The supply of drain voltage along with the additional gate-source voltage provides sufficient energy for the electrons to cross the potential barrier. Carrier mobilities in strained SiGe layer are different from that of Si [33] as a result of local distortion of band extreme due to strain effects, as well as due to the alloy scattering on the carriers. The mobilities in strained layer also depends on the transport direction, either parallel to the original SiGe growth interface or in the perpendicular direction [33]. In VESIMOS, on applying the bias, the electrons are transported towards the drain end and the holes are transported in the opposite direction towards the source end [21]. Fig. 7 shows the carrier concentrations (electron and hole) in different regions of the device.

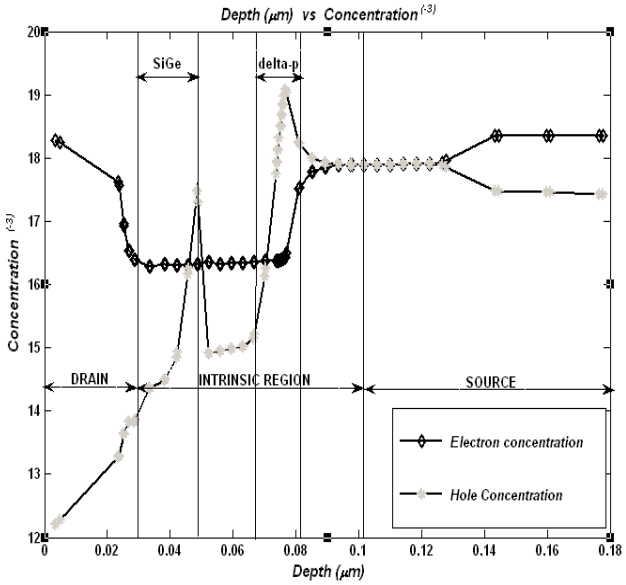

Figure 7. Electron and hole concentrations in different regions of the device.

It can be seen from fig. 7 that the electron concentration at the source end is higher than the hole concentration. This is due to the presence of n-type (Antimony) dopants in the substrate. On application of the bias, the electrons cross the p-type triangular barrier, and are transported towards the drain, thus forming the ON current of the device. The holes generated during the impact ionization process charge the floating p-body, and are transported towards the source end. However, electrons are the majority carries in VESIMOS. The carriers are transported through drift mechanism. Hence the drift current mechanism of carrier transport is seen in VESIMOS.

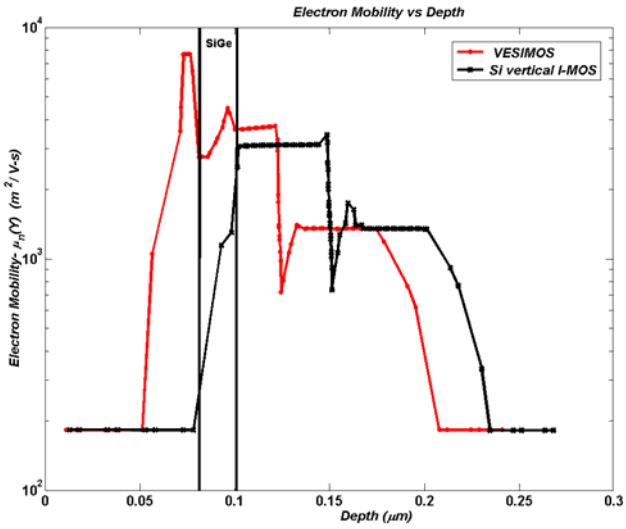

Figure 8. Comparison of electron mobility profiles of VESIMOS and relaxed Si vertical I-MOS.

A comparison between the electron mobility profiles, on application of bias, of both Si vertical I-MOS and VESIMOS were done as shown in fig. 8. It can be observed that the electron mobility is higher in the strained SiGe layer. The electron mobility in the strained $Si_{0.7}Ge_{0.3}$layer (~4200m^2/V-s), was found to be increased by 40% in comparison to relaxed Si vertical IMOS (3000 m^2/V-s). Due to the splitting of the valleys in conduction band into lower four-fold and higher two fold states, the electron mobility becomes dependent on the in-plane and out-of plane directions. In the in-plane direction (in the plane of growth), the heavy longitudinal electron mass leads to lower electron mobility, while, in the out-of plane direction (out-of plane growth), the effective electron mass is reduced and hence, the mobility increases. The higher doping levels also contribute to increase in electron mobility due to ionized impurity scattering [34]. However, alloy scattering in the strained SiGe layer, tends to affect the electron mobility [35]. Hence, as seen in figure 8, the mobility in the strained layer increases to a maximum value and then decreases. This is due to the alloy scattering of SiGe.

Fig. 9 shows the reduction in threshold voltages with increasing strain for various drain biases. At high strain, the bandgap reduction is higher. Hence, low threshold voltage value is obtained, such that for Ge = 50%, the threshold voltage is about 0.72V. In addition, the effect of strain on electron mobility was also analyzed, which revealed that, with increasing Ge content would increases the mobility of the electrons, linearly. Although with increasing strain would increases the mobility and reduces threshold voltage, it is not preferred to increase the strain much further, as it results in bandgap degradation [36].

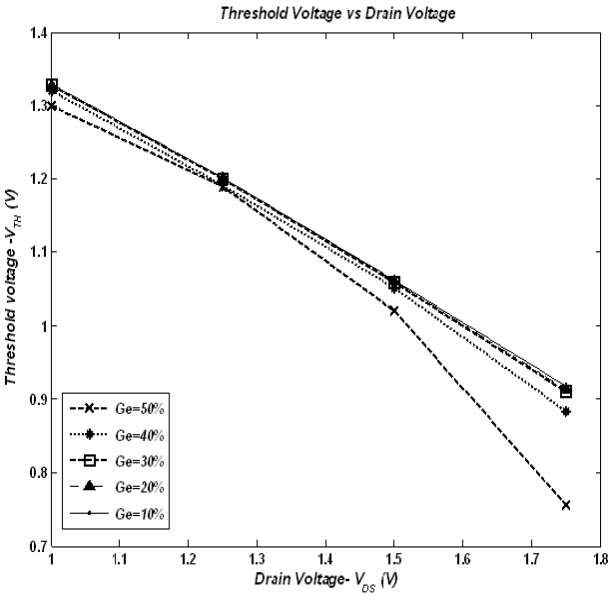

Figure 9. Variation of threshold voltage with Ge content.

Fig. 10 shows the variation of SiGe layer thickness on the threshold voltage. A threshold voltage increment of approximately 5-7% was observed, with increasing T_{SiGe} layer. This can be explained by the degree of strain relaxation (α)as a result of increasing thickness defined by equation 1.

$$\alpha = \frac{a_{SiGe(x)}(strained) - a_{Si}}{a_{SiGe(x)}(fullyrelaxed) - a_{Si}} \times 100 \quad (1)$$

Where $a_{SiGe(x)}$ is an average in-plane lattice constant of the strained epi SiGe layer, a_{Si} is the lattice constant of the substrate and $a_{SiGe(x)}$ is the average lattice constant of a fully relaxed SiGe layer. Thus, it shows that smaller α is obtained by increasing the compressive strain in the SiGe layer.

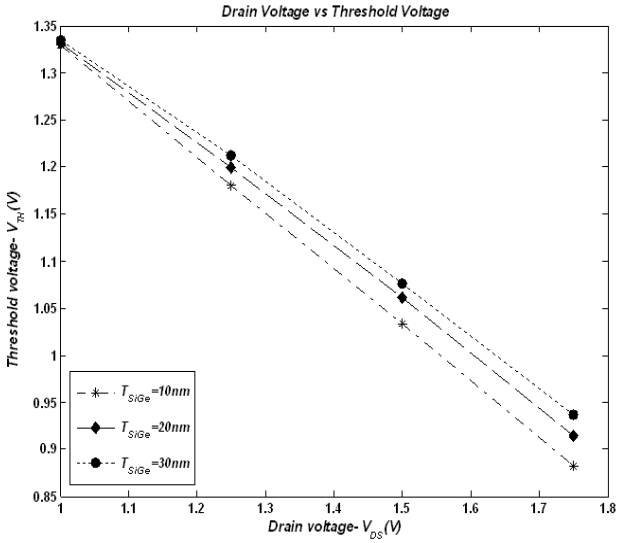

Figure 10. Variation of threshold voltage with $Si_{0.7}Ge_{0.3}$layer thickness.

Fig. 11 show the threshold voltage decreases with increasing doping concentration. This is in contrary to the doping effects of MOSFET, where the threshold voltage increases with increasing doping concentration. Hence, the I-MOS devices have this unique characteristic of showing reduced threshold voltages with increase in doping concentration. This effect was observed as a consequence of high electric field in the channel region [10], at high doping concentrations and hence, aids in reducing the threshold voltages.

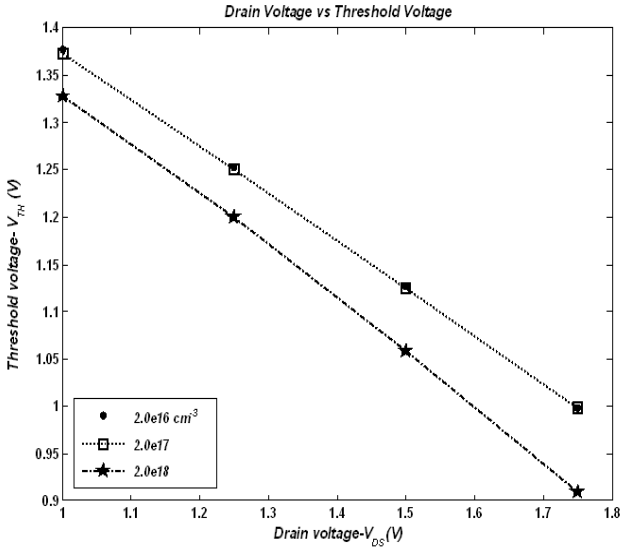

Figure 11. Variation of threshold voltage with Ge content.

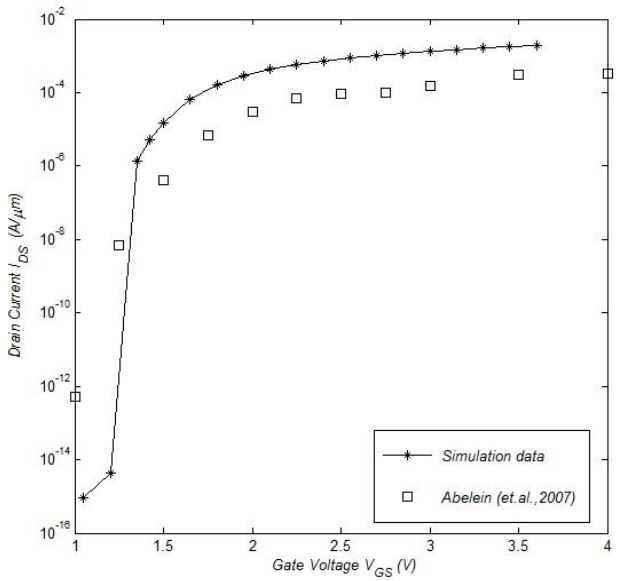

Figure 12. Validation of simulated data with experimental data (Abelein *et.al.*,2007) of Si vertical I-MOS device.

All simulated data was validated with experimental data in order to verify the accuracy of the simulation work. As no experimental data available for Vertical SiGe IMOS, the vertical Si IMOS data was used [15]. It can be observed that the simulated data is synchronous with the experimental data and is in close approximation of 0 to 5% range as shown in fig. 12.

IV. CONCLUSION

The superior performances of Vertical Strained-SiGe Impact Ionization MOSFET (VESIMOS) were successfully analyzed. VESIMOS device integrate vertical concept of IMOS device with strained SiGe technology. The electrical characteristics of the VESIMOS by varying the amount of strain, the strained layer thickness, and the S/D doping concentrations were obtained using Silvaco TCAD tools. Moreover, 40% improvement of electron mobility was revealed, besides an improvement in obtaining lower threshold voltage and supply voltage. The threshold voltage is better for VESIMOS (V_{TH}=0.88V) than the vertical Si IMOS and strained SiGe IMOS. The sub-threshold voltage (S=9.8 mV/dec) in VESIMOS is also lower than the Si-vertical IMOS (S=20mV/dec). The VESIMOS also shows good I_{on}/I_{off} ratio of 10^{12}. Based on these results, VESIMOS was projected as the most prominent candidate for nanoelectronics device.

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