Breakdown Voltage Reduction Analysis with Adopting Dual Channel Vertical Strained SiGe Impact Ionization MOSFET (VESIMOS)

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***Abstract*—The Single and Dual Strained SiGe layer for Vertical Strained Silicon Germanium (SiGe) Impact Ionization MOSFET (VESIMOS) have been successfully analyzed in this paper. It is found that the drain current for single (SC) and dual channel (DC) VESIMOS were increased sharply initially due to the presence of Germanium. Germanium has high impact ionization rates to ensure that the transition from OFF state to ON state is abrupt. However, breakdown voltage of the SC device was decreased from B_V=2.9V to 2.5V by increasing the composition of Ge from 10% to 30%. The same characteristics were found for DC VESIMOS where B_V= 2V had decreased to 1.6V by varying the Ge composition. In short, the breakdown voltage which affected by the appearance of the second SiGe channel and Ge composition was justified. Apart from that, with the presence of the second SiGe channel, the switching speed and I_{ON}/I_{OFF} of the device were improved. It was found that the sub-threshold slope of SC and DC VESIMOS were inversely proportional to the breakdown voltage.**

Keywords — Strained SiGe; Vertical Strained SiGe Impact Ionization MOSFET (VESIMOS); breakdown voltage; band gap

I. INTRODUCTION

Semiconductor device has been successfully scaled down over several decades with a better device performance and higher package density [1]. However, developers encounter a lot of challenges when the semiconductor devices beyond sub – 100 nm, such as sub-threshold slope swing, increased leakage current leading to high power consumption and heating [2]. At room temperature, sub-threshold slope of MOSFET was limited to 60mV/decade [3-5]. The bias voltage is directly proportional to the sub-threshold slope swing; whereby, sub-threshold slope was increased by scaling the bias voltage continuously. This lead to the leakage current increased exponentially meanwhile increasing the power consumption [6]. Impact ionization (II) MOSFET was introduced where drift mechanisms of carriers were applied instead of the diffusion method to solve the sub-threshold limitation [7-11]. Operation of IMOS required high drain voltage (V_{DS}) and it produced higher temperature. Due to higher temperature produced, hot carrier effects were occurring where the gate oxide of the MOS was destroyed by the electrons [12]. Vertical impact ionization MOSFET was introduced to overcome the hot carrier effect problem. Vertical IMOS did not based on the avalanche breakdown as lateral IMOS. Holes generated by II and it charges the floating p – floating to lead the drain current in the sub-threshold region increase rapidly. However, high demand on the supply voltage is required to operate the Vertical IMOS. In order to reduce the supply voltage, a strained SiGe was introduced near end of the drain channel. SiGe has a smaller band gap compare with the Silicon and higher impact ionization rates in this region [13-14]. Yet, ratio of silicon to germanium must be selected carefully to optimize the performance of the device [15]. However, one of the main limitations using strained SiGe is low breakdown voltage. The degradation of breakdown voltage will highly affect the short channel with threshold voltage roll-off and an increase in sub-threshold slope [16].

In this work, investigation of the transfer characteristic and output characteristic in single channel $Si_{1-x}Ge_x$ VESIMOS (SC VESIMOS) and dual channel $Si_{1-x}Ge_x$ VESIMOS (DC VESIMOS) was carried out successfully by using Silvaco's TCAD simulation tools. Enhancement of the electron mobility and the fraction of Ge will affect the performance of the VESIMOS in term of threshold voltage and sub-threshold swing. Besides that, increasing of the Ge mole fraction and the thickness of the strained layer will affect the breakdown voltage. Higher breakdown voltages are more favorable because it could maintain the lifetime of the device. Therefore, the degradation of the breakdown voltage is a highly important short channel effect of nano-scaled device.

II. REVIEW OF PREVIOUS WORKS

Transformation of transistor size from huge to nano size is fast according to the Moore's law. Since the year 1974, the density of transistor on a single chip has been increased to double every 18 months as well as the performance [27]. In 2011, the number of transistors on a single chip is approaching 1.3 billion [28]. There are several issues occurred included high sub – threshold slope swing, increase of leakage current and lead to high power consumption and heating when the size of transistor

reduces. Hence, Impact ionization Metal Oxide Semiconductor (IMOS) was first introduced by K. Gopalakrishnan in 2002 to clarify the issues occurred [6]. The structure of IMOS is based on the diode (PiN) design. PiN structure developed to express the breakdown voltage of IMOS device and it is based on the position of the gate in the intrinsic region, intrinsic lengths and the doping concentration level [7]. The working principle of IMOS is contingent on the impact ionization method. Impact ionization is a process of the charge carrier lost its energy and created an electron holes pair. There is a linkage of carrier's energy and gate voltage supply to the device. By increasing the gate voltage, the lateral electric field in the device will be increased and the device has undergone breakdown condition when achieves the critical field. Thus, the impact ionization is occurring in the device. By using the impact ionization concept, an exceptional achievement of sub – threshold slope is obtained which is approximately of 10mV/ decade [7]. However, IMOS required high voltage supply for breakdowns occur entail the hot carries degradation effects in the device [29].

Lateral IMOS still was suffering from the high operating voltage and damages by the hot electrons to the oxide [30]. In order to solve the problems, vertical IMOS was introduced by U. Abelein in 2007 and several experiments have been carried out [31]. Vertical IMOS is a planar doped barrier MOSFET with a floating body [32]. The basic operation of vertical IMOS is the holes generated by impact ionization and its charge the floating p-body and cause a dynamic reduction of threshold voltage [33]. Besides that, drain current of the device was increase rapidly in the sub – threshold region. The floating p-body is allocating in between the intrinsic region and near the contact region to allow high electric field to be achieved without high drain source voltage supplied. Furthermore, the leakage current observed in the experiment by U. Abelein *et.al* is extremely low which in the range of pA. Transfer characteristic of the Vertical IMOS has been observed by U. Abelein *et.al.* From the simulations, it found out the device can be operated in three different modes which is conventional MOSFET mode, impact ionization mode, and bipolar mode [32]. Vertical IMOS is operating in conventional MOSFET for the supply voltage less than 1.5V and the threshold voltage and sub – threshold slope swing observed in this region is 2.2V and 130mV/decade respectively. The sub – threshold slope swing for vertical IMOS in impact ionization mode is approximately 20mV/decade has been observed. Vertical IMOS was solved the hot carrier effects problem. However, it also has some limitations have been observed in the experiments which including the hysteresis problem [32] and switching speed problem [20]. The hysteresis problem can be explained by the parasitic bipolar transistor formed at high drain voltage with the drain region as emitter, source region as collector and delta layer as base. Bipolar transistor will deliver the electrons which provide the holes for its base current via impact ionization when the origin current of bipolar transistor exceed a limit and it could not turn off by reducing the gate source voltage. Therefore, a negative gate source voltage needs to be applied to the device to switch off. Vertical IMOS has a low switching speed issue where the floating body needs to be discharged completely through the body junction. However, there is a challenging to increase the switching speed for the vertical IMOS.

Vertical strained SiGe IMOS was introduced by Dinh T.V *et.al* to reduce the supply voltage to the device [14]. SiGe has a smaller band gap compare to the silicon where it has higher impact ionization rates will occur in the layer. A thin layer of strained SiGe was integrated in the intrinsic region near the drain. For optimized performance of the device, ratio of silicon to germanium, thickness of the SiGe layer, shape and position of the layer must be selected carefully [20]. Due to alloy scattering, ionization coefficient for the 20% mole fraction of Germanium in strained SiGe layer was found much smaller compared to silicon [20]. Threshold voltage of vertical strained SiGe IMOS has been improved 0.2V to 0.7V as observed by Dinh T.V *et.al.* A further analysis on transfer characteristic of strained vertical IMOS has been carried out by Divya *et.al* in 2012. A better threshold voltage and sub – threshold slope swing has been inspected by Divya *et.al*. Sub – threshold slope swing of 9.8 mV/decade and threshold voltage of 0.88V was recorded in the simulation [12]. Hence, the switching speed and the hysteresis problem have been solved. Notwithstanding, SiGe layer has exceptional potential to improve the electrical characteristics of the device. In this paper, second layer of strained SiGe layer has been allocated near the source region to investigate the performance of the device.

III. Device Structure

Figure 1 shows the detailed cross sections of the DCVESIMOS which was simulated for the device's performance by using Silvaco's package [17]. This structure comprises of an n+ doped drain region and source region, a SiGe layer is grown in the drain intrinsic zone and in the source intrinsic zone, a highly doped delta p+ layer in between the intrinsic region and double sided gates [18]. Formation of the SiGe layer at drain intrinsic region will cause the impact ionization to occur strongly [19]. However, highly doped delta p+ layer will create a potential barrier and without applying a high drain – source voltage, high electric fields can be achieved in the intrinsic zone near the drain.

IV. Device Simulations

The shape and thickness of the SiGe layer and the thickness of the P+ delta layer will affect the performance of the VESIMOS [20]. Therefore, an optimum thickness of the P+ delta layer and the doping concentration were selected to obtain quality sub threshold slope. Changes of the Germanium content will also affect the mobility in the device [21]. The strain level is related to the Ge mole fraction. The higher of the Ge mole fraction, the higher of the strain level obtained in the layer. Investigation of the performance of variation Ge Mole fraction from 10% to 50% for SCVESIMOS was successfully carried out. The

position of the SiGe layer needs to be determined carefully to achieve higher rates of the impact ionization in the drain intrinsic region.

VESIMOS was based on the impact ionization with the drift current mechanism concept, which involves high electric field. Doping concentration will affect the drift mechanism and the electric field in the VESIMOS. Therefore, a high doping concentration is required to obtain a better characteristic of the device. The source and drain were n-doped with Antimony and Phosphorus with a doping concentration of 2.1×10^{18} /cm^3 respectively. Doping concentration of P+ delta layer and intrinsic region are 1.0×10^{19}/cm^3 and 1.0×10^{19}/cm^3 respectively.

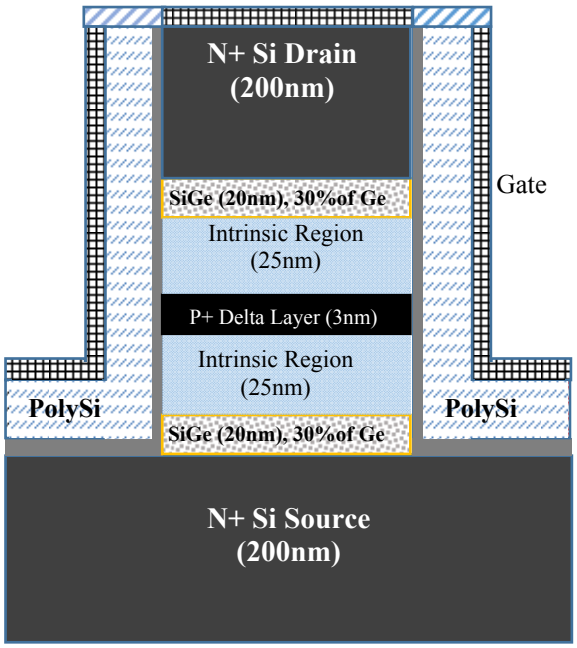

Fig. 1. Double layer SiGe VESIMOS device structure with dimension of L=40nm, d=200nm, respective thickness of the source, intrinsic region, P+ delta layer, SiGe layer, drain and both layer fractions of Ge is 30%.

Poisson's equation and continuity equation numerically can be done to investigate the electrical characteristics of the device within the explicit defined meshes [17]. By computing the Poisson's equation, it is allowed to observe the electrical potential energy and electronic band structures. Current densities of the electrons and holes can be calculated by using the continuity equations. The Boltzmann transport framework is used to solve the continuity equation and Poisson's equation. The self-consistent process will show the relationship between the current density of the electrons or holes and carrier concentration as well as the quasi-Fermi potential. Selberherr's model is a local impact ionization model [22]. Generally, Selberherr's model is employed for the device simulation, especially vertical impact ionization MOSFET. The drift – diffusion transport model with the Boltzmann carrier transport framework was applied to predict the transfer characteristic of the device.

V. Device Performance and Analysis

The performance of the VESIMOS was analyzed by invoking its output characteristic that examined by biasing the gate voltage, V_{GS} and ramping the drain voltage, V_{DS} at defined bias steps for both single and dual channel.

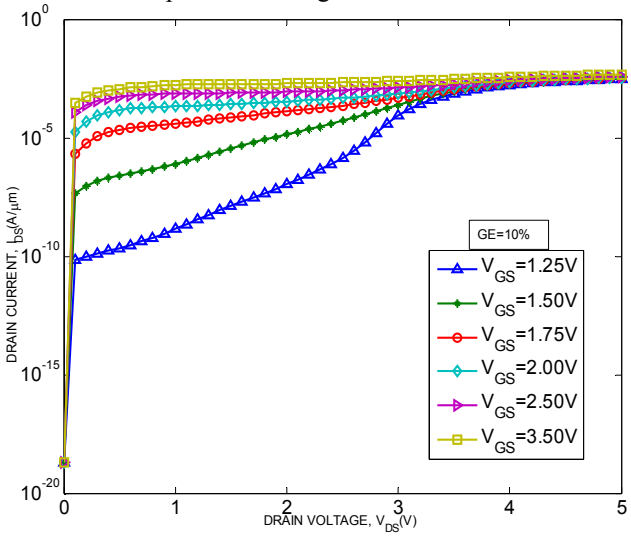

Fig. 2. Output Characteristics, I_D-V_D of SC VESIMOS for $Si_{0.9}Ge_{0.1}$ at different V_{GS}.

Figure 2 shows the output characteristic of SC VESIMOS with Ge=10% by supplying different V_{GS}. It can be seen that the drain current rises sharply initially, and then increase gradually, before going into saturation for V_{GS}<1.75V. Breakdown voltage was occurred at V_{DS}>3.5V. The same occurrences were also applied for SC VESIMOS with Ge= 20% and 30%. The sharp rise of initial drain current was attributed to the presence of Germanium. Germanium has a high and symmetric impact ionization rate, which ensures that the transition from OFF state to the ON state is abrupt [7].

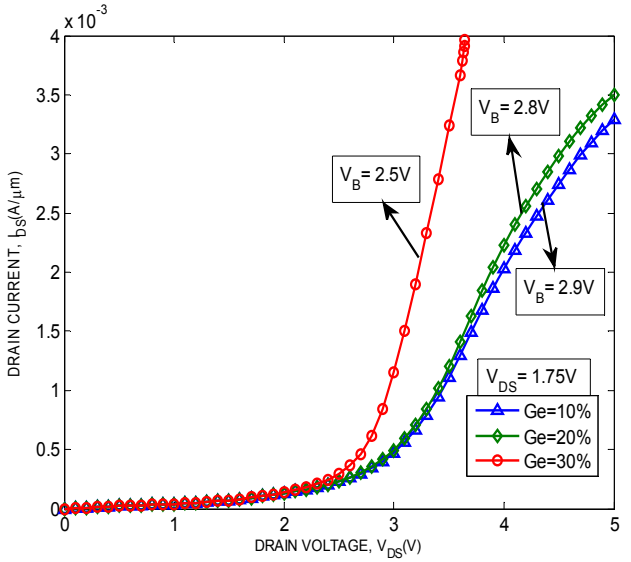

Fig. 3. Output Characteristics, I_D-V_D of variation Ge mole fraction for SC VESIMOS.

Figure 3 shows the output characteristics of SC VESIMOS with a variation of Ge mole fraction at

V_{GS}=1.75V. The breakdown voltage for Ge=10% is 2.9V, 2.8V when Ge=20% and the lowest breakdown voltage for Ge=30% is 2.5V. It can be seen that the breakdown voltage decreased the Ge mole fraction was increased. The same occurrences were also applied for DC VESIMOS at V_{GS}=1.75V as depicted in Figure 4.

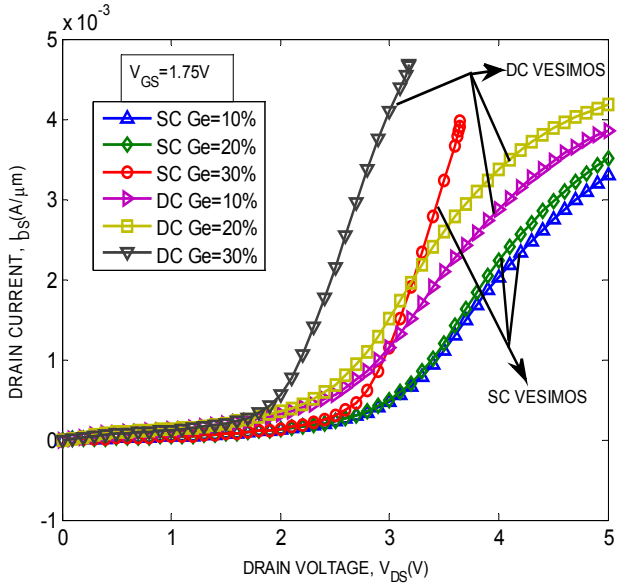

Fig. 4. Comparison of output characteristics, I_D-V_D of variation Ge mole fraction for SC and DC VESIMOS.

It shows that the DC VESIMOS breakdown voltage was lower compared to SC VESIMOS due to the appearance of the second layer of SiGe channel. The breakdown voltages were reduced rapidly by increasing the mole fraction of Ge with the appearance of the second channel. The low breakdown voltage of the device was lead to a lower band gap of the semiconductor materials and the breakdown voltage was also affected by the thickness of the materials [23]. Lower breakdown voltage is not beneficial because it could potentially reduce the lifetime of the device. However, fastest switching speed and lower I_{ON}/I_{OFF} ratio were obtained with presence of second channel SiGe.

There are three different modes in VESIMOS: conventional MOSFET, Impact Ionization (II), and Bipolar Junction Transistor (BJT) mode. The VESIMOS operation mode is based on the V_{DS} applied. The transfer characteristic is examined by biasing the drain voltage and ramping the gate voltage at defined bias steps for the SC and DC VESIMOS.

Figure 5 shows the comparison of the transfer characteristic between SC and DC VESIMOS with different Ge mole fraction at V_{DS}=1.75V. The SC VESIMOS is found to operate in conventional MOSFET due to the limited of drain supply voltage for electron to overcome the delta p+ potential barrier. However, DC VESIMOS is found to work in II mode due to sufficient energy was produced for creating electron hole pair. DC VESIMOS with Ge=30% has lowest sub-threshold slope value of S=10. 98mV/Dec and trifle higher threshold voltage compare to other devices. This significant result was due to dual channel strained layer with suitable Ge mole fraction that able to enhance the electron mobility based on the splitting of the valley [24].

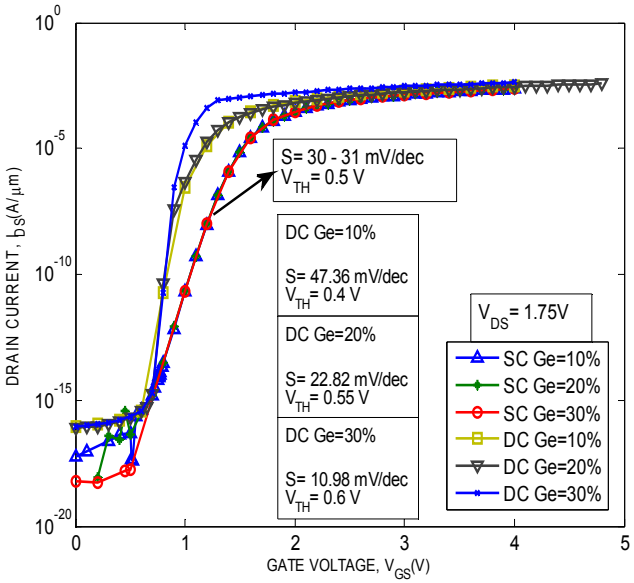

Fig. 5. Comparison of transfer characteristics, I_D-V_G of variation Ge mole fraction for SC and DC VESIMOS at V_{DS}=1.75V.

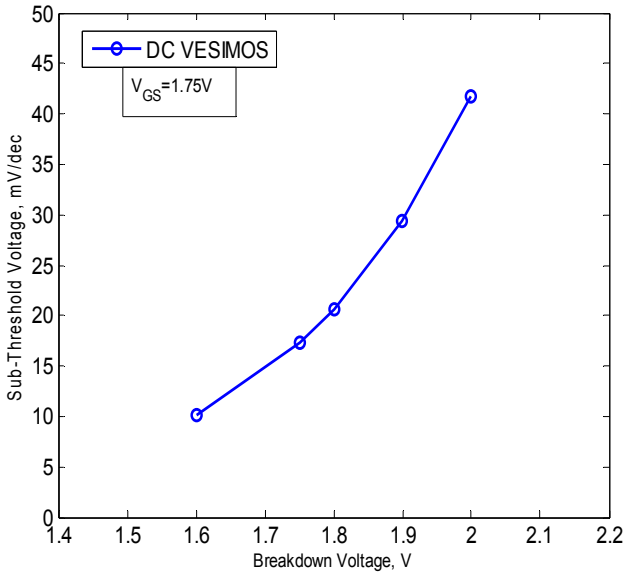

Fig. 6. Sub-threshold voltage versus breakdown voltage for DC VESIMOS.

Figure 6 revealed the relationship between sub-threshold voltage and breakdown voltage for SC and DC VESIMOS. It can be observed that the switching speed of the device was inversely proportional to the breakdown voltage for DC VESIMOS at V_{GS}=1.75V. The same occurrences were also applied for the SC VESIMOS. In the high drain region, higher breakdown voltage associated with suppression of the floating body effect in the SiGe region increased the hole flow to source region [25].

Table I summarize the performance comparison of SC and DC VESIMOS. It can be observed that the device's performance has improved in term of sub-threshold when increasing the Ge mole fraction for DC devices. The OFF

state current of DC devices is much smaller compare to SC devices with the appearance of the second SiGe layer.

TABLE I. PERFORMANCE COMPARISON OF SINGLE & DUAL STRAINED CHANNEL VESIMOS.

	SC	SC	SC	DC	DC	DC
Ge^1	10%	20%	30%	10%	20%	30%
Ge^2	-	-	-	10%	20%	30%
V_{TH} (V)	0.55	0.53	0.51	0.4	0.55	0.6
B_V (V)	2.9	2.8	2.5	2	1.8	1.6
S (mV/Dec)	31.4	30.64	30.61	47.36	22.82	10.98
I_{ON} (μA/μm)	10^{-3}	10^{-3}	10^{-4}	10^{-3}	10^{-3}	10^{-3}
I_{OFF} (μA/μm)	10^{-15}	10^{-15}	10^{-15}	10^{-16}	10^{-16}	10^{-16}
Ratio (I_{ON}/I_{OFF})	10^{12}	10^{12}	10^{11}	10^{13}	10^{13}	10^{13}

This significant result was due to the dual channel able to enhance the electron mobility to improve the I_{ON}/I_{OFF} based on the six fold degeneracy of the conduction band in the strained layer (Fig 7). The two fold shaded region is out-of plane valleys and the unshaded regions represent the four-fold in-plane valleys. The four-fold in-plane valleys are lowered below the two fold out-of plane valleys. The two out-of plane valleys are the lower transports mass which drop in energy and hence, the electrons move to populate these lower mass valleys [26].

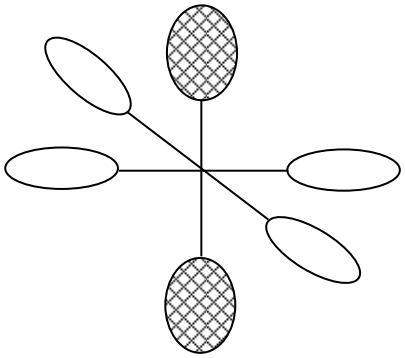

Fig. 3. Splitting of the six-fold degeneracy of the conduction band in compressively strained SiGe.

In order to decrease the OFF state current, it involved two main criteria, which are the energy gap and the drain voltage. Decreasing of the source voltage and smaller band gap energy were lead to the decrease the OFF state current. Several factors that result in reducing the breakdown voltage significantly are mainly due to low band gap energy, optimum thickness of composition layer, and the appearance of second layer.

IV. CONCLUSION

SC and DC VESIMOS were successfully been simulated and analyzed by using the TCAD simulation tools. It indicates that the breakdown voltage of the devices was affected by the composition of the Ge and the appearance of the second SiGe channel. However, with the presence of the second channel, it improved the sub-threshold slope and the OFF state current of the device. With lower band gap energy, optimum thickness of composition layer, and the appearance of second channel which lead to the improvement of the I_{ON}/I_{OFF}, it gives a great impact on the reduction of breakdown voltage remarkably.

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