Low-power and Wideband LC-VCO for WiMAX in CMOS Technology

Mohammed Aqeeli, Zhirun Hu, Xianjun Huang, Abdullah Albuaraikan, Cahyo Muvianto

School of Electrical and Electronic Engineering
The University of Manchester
Manchester, UK

mohammed.aqeeli-3@postgrad.manchester.ac.uk, z.hu@manchester.ac.uk, xianjun.huang@manchester.ac.uk, Abdullah.Albuaraikan@manchester.ac.uk, cahyo.muvianto@manchester.ac.uk

Abstract—This work presents an ultralow phase-noise and wide turning-range voltage-controlled oscillator (VCO) for 5.72GHz WiMAX applications. The fully integrated VCO is designed and simulated using 130-nm CMOS technology. Instead of using the conventional diode-based varactor in the tank design, high-performance body-grounded NMOS transistors are employed as effective varactors. A controlled self-biasing current source is implemented to avoid higher power supply sensitivity and higher up-conversion of flicker noise. The proposed VCO-measured results demonstrate a worst case phase noise of -132.6dBc/Hz at 1MHz frequency offset with an excellent figure of merit (FOM), which is -201.6dBc/Hz under a power consumption of 2.21mW. The VCO shows a tuning range of approximately 37.59%.

Keywords—CMOS; CMOS processes; Body-grounded NMOS varactor; current source; (MOM) capacitor; figure of merit; low phase noise.

I. INTRODUCTION

The recent exponential growth and higher integration of wireless communication has attracted remarkable efforts to develop more channels in mobile communication applications. The IEEE.16 unlicensed band of Worldwide Interoperability for Microwave Access (WiMAX), which refers to interoperable operations of the IEEE 802.16 for wireless-networks standards approved by the Windex Forum, provides fixed and portable wireless broadband connectivity independent of a base station. Three spectrum bands are adapted for global deployment, one of which is the unlicensed band (5.725-5.850)GHz.[1]. Nowadays, the demand for high-performance VCOs has increased, and consequently this demand has imposed stricter requirements on VCO phase noise. Phase noise can be triggered by a number of conditions, but it is mostly affected by VCO frequency stability, which is one of the most important parameters for the quality and performance of information transfer and in turn affects reliability in data communication[2]. P-N junction varactors[3], body-biased PMOS varactors[4] and switched capacitor arrays[5] are different approaches which are used widely to increase the bandwidth of VCOs design. Owing to the implemented techniques, the bandwidth and the phase noise of the VCO is substantially improved. However, PN junction present a narrower tuning range, large power dissipation is still unavoidable due to the stacking of body-biased PMOS transistors and additional noise appears because of the use of capacitor array switches.

High-performance LC-VCOs is a major challenge and require low-phase noise, low-loss and a wide tuning range varactors and sophisticated current biasing source. To achieve this object, the present work utilizes body-grounded NMOS devices as varactors to obtain high quality factor and better capacitance range and so better phase noise. In addition, a newly controlled current biasing source is designed to avoid higher power supply sensitivity and higher up-conversion of flicker noise. Furthermore, an improve phase noise property of VCO is achieved by implementing Metal-Oxide-Metal (MOM) capacitors in the tank of the VCO taking advantage of their high quality factor, high capacitance density, low parasitic capacitance, narrow spacing and thinner dielectric layers. This paper is organized as follows. Section II explains the VCO’s core design and the implementation process, while Section III presents the implementation and the measured results, followed by the conclusion in Section IV.

II. VCO DESIGN AND IMPLEMENTATION

The schematic diagram and the layout of the proposed VCO are shown in Fig. 1. The prime design considerations for the proposed VCO aim at improving tuning range and phase noise. For the tank circuit, body-grounded NMOS varactors are employed instead of PMOS or common PN-junction varactors. In order to implement a wide LC-VCO tuning range, it is important to decrease the number of parasitic capacitors. In this design, NMOS transistors are chosen due to the fact that parasitic capacitors in an NMOS pair are fewer than in a PMOS pair due to the smaller transistor size. Therefore, for the same value of gm, the W/L of an NMOS cross-couple is approximately one-third of a PMOS cross-couple. Also importantly, the proposed design utilizes a direct bias current source rather than the conventional mirrored bias current. The bias current of the VCO, which is an important parameter for phase noise optimization, is designed to handle the maximum current allowed by the specifications.

A. Body-grounded NMOS varactor in 130nm CMOS

Implementing (VCOs) in standard complementary metal oxide semiconductor (CMOS) technology is a major challenge for the design of radio-frequency (RF) transceiver integrated circuits (ICs). MOS devices in VCOs can produce wider tuning range, better Q and lower phase noise than diode varactors.
This new varactor mode is referred to as body-grounded NMOS varactor. Since the tuning voltage and the common
mode point are both $V_{dd}$ referred, supply noise is not coupled
into the tank by the varactor back gate capacitance and the VCO has excellent supply. The current biasing source,
maintain a constant large signal tank swing across NMOS varactors, thereby producing a constant common mode point
from a constant current into a constant tank resonate impedance[3]. In the proposed body-grounded varactor, four
pairs of symmetrical NMOS varactors are formed with 64
gate fingers. If the voltage $V_{GS}<V_{TH}$, an inversion zone is
established. The minimum value $C_{min}$ is reached when the
difference between electrodes is equal to the
threshold voltage $V_{TH}$. The maximum capacitance value per
unit of area, $C_{max}$ is equal to $E/\alpha_{ox}$ which corresponds to a
high accumulation value under the gate oxide. The tuning
range is defined by the ratio between $C_{min}$ and $C_{max}$.
According to the Cadence virtuoso analogue simulation
results, each pair of varactors alters capacitance from 0.25 to
0.70 pF as tuning voltage varies from 0 to 2.5V.

C. Self-biasing current source

A new controlled current source is designed specifically
for the proposed VCO to achieve optimal phase noise and
well-balanced differential outputs but with less power
consumption. The tail current reference source is designed
to generate current independently of the supply voltage
because of the high impedance element which has the ability
to overcome any possible variations. The current mirror is
formed by PMOS transistors (M3, M6) developing current
in the two branches of the circuit. The start-up circuit is
used to inject current and to move the current source from
the zero condition to the point of operation. By adjusting
resistor $R1$, the circuit will generate the suitable current for
the VCO. This current source is optimized properly to
reduce swing and as a result decrease phase noise even
more, in which case the circuit consumes less than 150
mA.

To sustain the oscillation, the higher the $g_m$ must be,

$$g_m \geq \frac{RC}{L}$$

The minimum biasing current, $I_{bias}=2I_D$ is inversely
proportional to the transconductance efficiency and the
inductance value and its quality therefore:

$$I_{bias} \geq \frac{2}{\sqrt{L/C_{core}+4C_{par}}} 1/\alpha_{ox}$$

Taking into consideration all of the parasitic mostly
associated with the tank of the VCO’s, the frequency of
oscillation can be derived as:

$$\omega = \frac{1}{\sqrt{L(C+C_{par}+4C_{par})}} \left[ -\frac{R^2(C+C_{par}+4C_{par})}{L} \right]$$
\[ I_{bias} = \frac{g_m}{I_D} \left( \frac{2}{Q_f \sqrt{(C + C_{gs} + 4C_{po})}} \right) = 1.84mA \]  \hspace{1cm} (4)

In this work we can calculate the minimum required biasing current from (4). From this equation it can be seen clearly that transistor capacitance C requires a decrease in the C value compared with the ideal case for a given resonant frequency. This equation establishes the importance of MOSFET size, and the result is that the bigger it is, the higher the \( g_m \) must be to achieve oscillation.

D. Center taped inductor

The proposed inductors turned out to be near optimum for the oscillator design goal of reducing the internal series resistor. Relatively small \( L \) and high Q inductor values are key to a high-performance, low-power and low-noise oscillator. In this work, the designed inductor is a symmetrical center-tapped inductor, taken into consideration by obtaining the maximum Q factor at 5.72 GHz. It was simulated at different frequencies, as shown in Fig. 2, and the measured quality factor \( Q \) was 18.10 for 359 pH inductors, while the area was 15190 \( \mu \)m. For the planner inductor, value \( L \) can be given approximately by (5):

\[ L = \frac{\mu_0}{2\pi} \left( \ln \left( \frac{l}{n(t+w)} + 0.2 \right) \right) \]  \hspace{1cm} (5)

The total length of the winding (l) is:

\[ l = (4n+1)r + 9(N+1)N(w+s) \]  \hspace{1cm} (6)

where \( s \) is winding spacing, \( t \) is the thickness of the material, \( n \) is the winding count, \( w \) is the winding width, \( N \) is integer \((n)\), \( \sigma \) is the conductivity of the interconnect, \( \delta \) is skin depth and \( \mu_0 \) is magnetic permeability.

E. MOM capacitors

VCOs depend only on technology-dependent factors, in other words on the Q of inductor(s) and capacitors. Integrated inductance-capacitance (LCs) are standard components in LC tank VCO circuits and may become the most important part of a high-performance VCO circuit design. VCOs use various types of integrated capacitors utilizing MOS, p-n junctions, MIM (metal-insulator-metal), poly-to-poly, MOM and other structures. MOM capacitors are one of the most widely used, due to their high capacitance density, low parasitic capacitance, symmetrical plate design, superior RF characteristics and no additional masks or process steps – and thus low cost.

In symmetric-type MOM structures, the architecture consists of two ports, and the number of fingers per layer is limited to even numbers, in order to maintain symmetry. There are six metal layers, finger length (\( L_f \)) is 12 and the area is 424.36\( \mu \)m². Fig.3 illustrates simulated frequency dependent quality factor of MOM capacitor designed with a 130nm CMOS process technology.

III. SIMULATION RESULTS

The demonstrated VCO generates stable periodic signals with a harmonic index and measured output power of 5.73dBm at the resonance frequency, as shown in Fig. 4.
By implementing body-grounded NMOS varactors, the VCO can significantly increase the tuning range from (4.62-5.68)GHz to (4.63-6.78)GHz. This provides up to 19.23% better performance than the conventional NMOS varactors and approximately 12% better than the body-biased PMOS varactors as shown in Fig. 5, with tuning voltage varying from 0 to 2.5 V. The solid and the dotted lines represent simulation results using NMOS varactors with and without body-grounding.

Fig. 5. Output frequency of the designed VCO

Generally, random FM walk noise is an enduring component in oscillator phase noise [6]. This component seems to be unnoticeable because the component, which is up-converted from the flicker noise in active devices and current sources, significantly outweighs random FM walk noise. However, since the proposed circuit design can reduce flicker noise in MOSFETs, FM flicker noise is kept to a minimum. The phase noise of an LC-VCO is described, according to Leeson, as [7]

\[
L(f_o) = 10 \log \left[ \frac{1}{2} \left( \frac{f_o}{2f_c Q} \right)^2 + 1 \right] \left( \frac{f_o}{f_c} + 1 \right) \left( \frac{F K T}{p_i} \right)
\]

Fig. 6 shows the phase noise measurement results at 5.72 GHz, for which the SSB phase noise measured at 1 MHz offset from the carrier frequency were -132.68dBc/Hz. By using a 1.2 V supply voltage, the total power consumption of the VCO core is 2.21 mW. To compare the performance of previously published oscillators and the FOM, we used the model adopted by Ham and Hajimiri[8], which normalizes the measured phase noise with respect to center frequency and power consumption. It is defined by equation (8):

\[
FOM = L(f_c) - 20 \log \left( \frac{f_o}{f_c} \right) + 10 \log \left( \frac{P_d}{1mW} \right)
\]

Table 1: Performance Comparison of CMOS VCOs

<table>
<thead>
<tr>
<th>Process</th>
<th>F (GHz)</th>
<th>P (mW)</th>
<th>PN(dBc/Hz)</th>
<th>Offset</th>
<th>TR(GHz)</th>
<th>FOM(dBc/Hz)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.09µmCMOS</td>
<td>5.63</td>
<td>14.00</td>
<td>-108.50</td>
<td>1.0</td>
<td>4.50-7.10</td>
<td>-172.00</td>
<td>[9]</td>
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<tr>
<td>0.18µmCMOS</td>
<td>5.20</td>
<td>9.70</td>
<td>-113.70</td>
<td>1.0</td>
<td>4.39-5.26</td>
<td>-180.00</td>
<td>[10]</td>
</tr>
<tr>
<td>0.18µmCMOS</td>
<td>6.00</td>
<td>12.50</td>
<td>-115.50</td>
<td>1.0</td>
<td>5.72-6.02</td>
<td>-179.80</td>
<td>[11]</td>
</tr>
<tr>
<td>0.18µmCMOS</td>
<td>5.80</td>
<td>10.08</td>
<td>-117.00</td>
<td>1.0</td>
<td>5.27-6.41</td>
<td>-184.00</td>
<td>[12]</td>
</tr>
<tr>
<td>0.18µmCMOS</td>
<td>5.10</td>
<td>9.70</td>
<td>-122.40</td>
<td>1.0</td>
<td>4.80-5.40</td>
<td>-152.00</td>
<td>[13]</td>
</tr>
<tr>
<td>0.25µmCMOS</td>
<td>4.77</td>
<td>18.18</td>
<td>-122.10</td>
<td>1.0</td>
<td>3.60-4.77</td>
<td>-184.90</td>
<td>[14]</td>
</tr>
<tr>
<td>0.18µmCMOS</td>
<td>6.98</td>
<td>3.40</td>
<td>-108.10</td>
<td>1.0</td>
<td>6.54-6.98</td>
<td>-180.00</td>
<td>[15]</td>
</tr>
<tr>
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<td>3.95</td>
<td>6.60</td>
<td>-147.00</td>
<td>10.0</td>
<td>3.40-4.50</td>
<td>-191.00</td>
<td>[16]</td>
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<tr>
<td>0.13µmCMOS</td>
<td>5.72</td>
<td>2.21</td>
<td>-132.68</td>
<td>1.0</td>
<td>4.63-6.78</td>
<td>-201.60</td>
<td>This work</td>
</tr>
</tbody>
</table>

F: Frequency, P: power, PN: Phase noise, TR: Tuning range, FOM: Figure of Merit.
Table I summarizes measured performance, where the figure of merits with tuning range is used for comparison between this work and other state-of-the-art CMOS applications. Phase noise automatically decreases, while power consumption is reduced; thus, there is a trade-off between power consumption and phase noise[6].

IV. CONCLUSIONS

A general design methodology for low-power and wideband LC-VCO with body-grounded NMOS varactors is proposed to reduce the flicker noise, and meanwhile increase the tuning range. Moreover, the self-biasing current source circuit avoids two major disadvantages; higher power supply sensitivity and higher up-conversion of flicker noise. It is shown that optimization will yield a trade-off between phase noise and power consumption. As proof of the concept, the overall measured worst-case phase noise was -132.68dBc/Hz at a 1 MHz frequency offset, approximately over the whole working band. As a result, this CMOS VCO achieves a best FOM of -201.60dB. The VCO shows an approximate 37.59% tuning range. The VCO is tuned from (4.63-6.78) GHz with a tuning voltage varying from 0 to 2.50 V and a power dissipation of only 2.21 mW. Importantly, the proposed NMOS VCO design demonstrates very low phase noise and approximately fixed values at all tuning range due to the high quality LC-tank components and the direct bias current source.

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