Single Input Multi Output Digitally Reconfigurable Biquadratic Analog Filter

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Abstract—In this paper, a digitally re-configurable Single Input Multi Output voltage mode multifunctional biquadratic analog filter has been presented. The circuit realizes a Single Input Multi Output filter with non-inverting High Pass, Band Pass and Low Pass outputs and employs four Differential Voltage Current Conveyor blocks and uses seven passive components which are two grounded capacitors and five grounded resistors. Digital controlling is incorporated using a current summing network. Tuning of cut-off frequency is carried out with the help of a 3-bit digital control word (k). PSPICE simulations using TSMC 0.25 micron CMOS technology have been performed to validate the theoretically predicted results.

Keywords—Voltage-mode; Differential Voltage Current Conveyor (DVCC); multifunctional filter; digitally programmable circuits; Current Summing Network (CSN); Single Input Multi Output (SIMO).

I. INTRODUCTION

With the emerging technologies current mode circuits came as a new and more efficient analog building blocks. Current mode circuits provide various advantages over the conventional voltage mode circuits like wider bandwidth, greater linearity, higher slew-rate, better dynamic range, simple circuitry and low power consumption [1]. Thus current mode circuits soon became popular choice for various high frequency analog signal applications. The most significant of them are in the realization of analog filters and oscillators [2].

CCII (Second Generation Current Conveyor) which was introduced by Sedra and Smith proved to be the most popular and successful [3]. But it was unable to give differential or floating inputs which were demanded by various applications like impedance converter circuits and current-mode instrumentation amplifiers which require two high input impedance terminals. Also these applications used floating elements to minimize the number of CCII blocks used. These demands give rise to a new building block called a differential difference current conveyor (DDCC) which was presented in 1996 [4]. Later in 1997, a novel differential voltage current conveyor (DVCC) building block was given as a modification in DDCC block. DVCC was actually DDCC having its Y3 terminal grounded [5]. This versatile analog building block, the DVCC is now becoming more popular and several works are being done in this field. Some of the recent works in this field includes a DVCCs Based High Input Impedance Voltage-Mode Multifunctional filter by Jiun-Wei Horng in which the all-pass, high-pass and low-pass signals can be obtained simultaneously from the circuit configuration [6]. Later Hua-Pin Chen, Kuo-Wei Huang, and Po-Ming Huang introduced a DVCC-Based voltage-mode First-Order Filter which simultaneously realized low-pass, high-pass and all-pass filter responses from the same configuration using lesser number of active and passive components [7]. Recently Iqbal A. Khan and Ahmed M. Nahhas presented a digitally controlled current conveyor that has been used to realize a digitally controlled voltage mode first order multifunctional filter [8].

In this paper the circuit proposed in [9] by Tarek M.Hassan, A.M. Soliman employing four DVCC blocks, two grounded capacitors and five grounded resistors has been used to design and implement a digitally reconfigurable voltage-mode multifunctional biquadratic filter. High-pass, Band-pass and Low-pass filter responses can be obtained simultaneously without changing the circuit topology. This further enhances the circuit utility and usage by reducing the overall cost of the circuit. As the grounded capacitor in a circuit can compensate for the stray capacitances at that node thus the use of grounded capacitors in this topology makes the circuit suitable for integration. PSPICE simulations of the CMOS based programmable filter are performed to demonstrate results.

II. DIFFERENTIAL VOLTAGE CURRENT CONVEYOR

The Differential Voltage Current Conveyor (DVCC) block is as shown in the Fig.1. It is an active building block having five-terminals whose terminal characteristics can be described by the following matrix equation [10]:

\[
\begin{bmatrix}
I_{Y1} \\
I_{Y2} \\
V_X \\
I_Z \\
I_Z
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
1 & -1 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 \\
0 & 0 & -1 & 0 & 0 \\
\end{bmatrix}
\begin{bmatrix}
V_{Y1} \\
V_{Y2} \\
I_X \\
V_{Z1} \\
V_{Z2}
\end{bmatrix}
\]

(1)

While the X terminal voltage \(V_X\) follows the voltage difference of terminals Y1 and Y2 \((V_{Y1} - V_{Y2})\), the output currents \(I_Z\) and \(I_Z\) follow the input current injected at the X terminal \(I_X\), where \(I_Z\) is the positive-type output current and \(I_Z\) is the negative-type.
An ideal DVCC exhibits negligible or almost zero input resistance at the terminal X whereas both the Y terminals as well as the Z terminal have very high ideally infinite resistance. The current flow direction at the input and the output terminals is such that either both currents flow into or out of the device. The CMOS implementation of DVCC is as shown in Fig. 2.

The implemented voltage-mode multifunctional filter [9] is shown in Fig. 3.

Analysis of the circuit gives, the following transfer functions:

\[
\frac{V_{HF}}{V_i} = \frac{s^2R(R_3 + R_4)}{s^2 + \frac{R}{R_1R_4C_1} + \frac{R}{C_1C_2R_1R_2R_3}}
\]  

(2)

\[
\frac{V_{LP}}{V_i} = \frac{R(R_3 + R_4)}{s^2 + \frac{R}{R_1R_4C_1} + \frac{R}{C_1C_2R_1R_2R_3}}
\]  

(3)

Here the resonant angular frequency (\(\omega_0\)) and the quality factor (Q) are given as:

\[
\omega_0 = \sqrt{\frac{R}{R_1R_2R_5C_1C_2}}
\]  

(5)

\[
Q = \frac{R_4C_1}{\sqrt{RR_2R_5C_2}}
\]  

(6)

We can see that high-pass, band-pass and low-pass functions can be realized simultaneously at different terminals without changing the circuit topology. In simulations, using PSPICE the DVCC was realized by the CMOS implementation as shown in Fig. 2 using TSMC 0.25-μm process parameters. Aspect ratios of the CMOS transistors of the DVCC are presented in Table I.

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W (μm)</th>
<th>L(μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M4</td>
<td>1</td>
<td>0.8</td>
</tr>
<tr>
<td>M5-M6</td>
<td>24.2</td>
<td>0.8</td>
</tr>
<tr>
<td>M7-M8</td>
<td>6.8</td>
<td>0.8</td>
</tr>
<tr>
<td>M9-M11, M17</td>
<td>18.6</td>
<td>0.6</td>
</tr>
<tr>
<td>M12-M14</td>
<td>25</td>
<td>0.8</td>
</tr>
<tr>
<td>M15</td>
<td>19.6</td>
<td>0.8</td>
</tr>
<tr>
<td>M16</td>
<td>18</td>
<td>0.8</td>
</tr>
<tr>
<td>M19</td>
<td>20</td>
<td>0.6</td>
</tr>
</tbody>
</table>
\( V_{DV} = -V_{SS} = 2 \text{ V} \) are the supply voltages and \( V_{B1} = -1.32 \text{ V} \) and \( V_{B2} = +0.7 \text{ V} \) are the two biasing voltages. The circuit was designed for \( f_0 = \frac{\omega_0}{2\pi} = 795.8 \text{ kHz} \) and \( Q = 8 \) by choosing \( R_2 = R_3 = 0.5 \text{ k}\Omega, R_1 = R_4 = 2 \text{ k}\Omega \) and \( C_1 = C_2 = 0.2 \text{ nF} \). The responses of the above given filter design are shown in Fig. 4 and the results are in accordance with the theoretical analysis.

IV. DIGITALLY CONTROLLED DVCC

To introduce the re-configurability in the multifunctional filter we have used a digitally controlled DVCC (DC-DVCC). The modified terminal characteristics for the same are as follows:

\[
\begin{bmatrix}
I_{Y1} \\
I_{Y2} \\
V_X \\
I_{Z+} \\
I_{Z-}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
1 & -1 & 0 & 0 & 0 \\
0 & 0 & k & 0 & 0 \\
0 & 0 & -k & 0 & 0
\end{bmatrix}
\begin{bmatrix}
V_{Y1} \\
V_{Y2} \\
I_X \\
V_{Z+} \\
V_{Z-}
\end{bmatrix}
\]

For obtaining the digital control in the DVCC current summing networks (CSNs) are employed at the \( Z \) (\( Z^+ \) and \( Z^- \)) terminals for controlling the current transfer gain parameter \( k \) which can be varied from 1 to \( (2n - 1) \). This \( n \) represents the number of transistor arrays.

Where:

\[ k = \frac{I_Z}{I_X} \]

The modified circuit of DVCC with the transistors arrays is as shown in Fig. 5. The CSN consists of \( n \) transistor pairs, the aspect ratios of whose PMOS and NMOS transistors respectively are given by:

\[
\begin{bmatrix}
\frac{W}{L}
\end{bmatrix}_i = 2^i \begin{bmatrix}
\frac{W}{L}
\end{bmatrix}_1 \]

(8)

\[
\begin{bmatrix}
\frac{W}{L}
\end{bmatrix}_i = 2^i \begin{bmatrix}
\frac{W}{L}
\end{bmatrix}_{12} \]

(9)

Furthermore, the current at the output terminal (\( Z \)), is assumed to be flowing out of the DC-DVCC and can expressed as:

\[ I_Z = \sum_{i=0}^{n-1} d_i 2^i (I_9 - I_{12}) \]

(10)
Therefore, the proposed DC-DVCC provides a current transfer gain, $k$ equal to:

$$k = \frac{I_Z}{I_X} = \frac{\sum_{i=0}^{n-1} d_i 2^i (I_9 - I_{12})}{(I_9 - I_{12})} = \sum_{i=0}^{n-1} d_i 2^i$$  \hspace{1cm} (11)

Where $d_i$ are the bits applied to the $i$-th branch in the CSN. Current flow in a particular branch is enabled or disabled depending upon whether $d_i$ is a logic 1 or logic 0 [12].

V. DIGITALLY RE-CONFIGURABLE MULTIFUNCTIONAL FILTER

In this section the proposed digitally re-configurable voltage-mode multifunctional biquadratic filter has been presented as shown in Fig. 6. Here two of the DVCC blocks are replaced by the DC-DVCC blocks and are digitally controlled using the 3-bit control word, $k$. The introduction of the DC-DVCC comprising of CSN modifies the expression of pole-frequency $\omega_0$ of the multifunctional filter. The expressions for the digitally reconfigurable filter responses can now be expressed as:

$$\frac{V_{HP}}{V_i} = \frac{s^2 R (R_3 + R_4)}{R_3 R_4}$$  \hspace{1cm} (12)

$$\frac{V_{BP}}{V_i} = \frac{s k R (R_3 + R_4)}{R_3 R_4 C_1 R_3 R_4}$$  \hspace{1cm} (13)

$$\frac{V_{LP}}{V_i} = \frac{k^2 R (R_3 + R_4)}{R_3 C_1 R_2 C_3 R_3 R_4}$$  \hspace{1cm} (14)
The modified resonant angular frequency \( \omega_0 \), is given by:

\[
\omega_0 = k \sqrt{\frac{R}{R_1R_2C_1C_2}}\quad (15)
\]

VI. SIMULATION RESULTS

The proposed digitally re-configurable multifunctional biquadratic filter circuit in Fig.6 has been simulated and all the results are verified using PSPICE. Fig. 7, 8 and 9 shows the simulated responses obtained for the high-pass, band-pass and low-pass filters respectively keeping the digital control word \([d_2\;d_1\;d_0] = [0\;1\;0]\) and \([1\;0\;0]\). The 3-bit digital control word is varied from \([0\;0\;1]\) to \([111]\) to obtain the variation in the cut-off frequency of the multifunction filter and the results are reported in the Table II. It is also to be noted that only digital the control word is varied to obtain the variation in the cut-off frequency without changing the value of any of the passive components i.e. resistors and capacitors being used in the design. Fig.10 (a), (b) and (c) are the plots showing the variation in the cut off frequency with the control word.

Fig. 7(a). Simulated magnitude response (in dB) for high-pass filter with \([d_2\;d_1\;d_0 = 0\;1\;0]\) control word selected

Fig. 7(b). Simulated magnitude response (in dB) for high-pass filter with \([d_2\;d_1\;d_0 = 1\;0\;0]\) control word selected

Fig. 8(a). Simulated magnitude response (in dB) for band-pass filter with \([d_2\;d_1\;d_0 = 0\;1\;0]\) control word selected

Fig. 8(b). Simulated magnitude response (in dB) for band-pass filter with \([d_2\;d_1\;d_0 = 1\;0\;0]\) control word selected

Fig. 9(a). Simulated magnitude response (in dB) for low-pass filter with \([d_2\;d_1\;d_0 = 0\;1\;0]\) control word selected

Fig. 9(b). Simulated magnitude response (in dB) for low-pass filter with \([d_2\;d_1\;d_0 = 1\;0\;0]\) control word selected
VII. CONCLUSION

In this paper, a SIMO based digitally reconfigurable voltage-mode multifunctional biquadratic filter was presented. Digital control has been obtained by the variation of 3-bit digital control word using a Current summing network (CSN). As a result we got a multifunctional biquadratic filter which can provide high-pass, band-pass and low-pass filter responses of varying cut-off frequencies simultaneously from different output terminals without any change in the passive elements. Further we got linear variation in the cut-off frequency with the control word. PSPICE simulations were carried out to verify its working and are found to be in full agreement with theoretical expectations.

VIII. REFERENCES