A Novel Power Efficient 12T Full Adder

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***Abstract* - With continuous scaling of technology, density of transistor is increasing which leads to higher power dissipation on the chip. Therefore the need of the hour is to reduce the power consumption of individual circuits. In this paper a new a power efficient 12 transistor adder circuit is proposed. A twisted diode connection of transistor is used to reduce the power consumption in this work. The proposed adder is operated at 1V supply with 1.894 µW in 90 nm TSMC CMOS process technology.**

Keywords - Adder, CMOS, SERF, power.

I. INTRODUCTION

Addition is a basic arithmetic operation and fundamental in use of Arithmetic Logic Unit and hence microprocessors and Digital Signal Processing Units. Addition forms a basis for other operations like subtraction, multiplication division etc. Therefore area and power optimized adder circuits are the essence of processing units of all currently used gadgets.

Symmetric Adder is the most fundamental adder and uses 28 transistors. Recent work has proposed Adders with lower number of transistors [1]-[5.] With increasing number of transistors on the chip, power has become an issue and several techniques have been proposed to reduce power [6]. A number of techniques are used to reduce the power by lowering the signal swing.

Three major sources comprises to power dissipation in digital circuits

$$P = p_t f_c\left(C_L V_{DD} V_{sig}\right) + \left(I_{SC} V_{DD}\right) + \left(I_{leakage} V_{DD}\right) \quad (1)$$

Where $p_t f_c\left(C_L V_{DD} V_{sig}\right)$ = switching power,

$I_{SC} V_{DD}$ = short circuit power

$I_{leakage} V_{DD}$ = Leakage power.

For the dynamic power component $p_t f_c\left(C_L V_{DD} V_{sig}\right)$, every input transition from '0' to '1' or vice versa leads to switching activity at the output depending on the input combinations. If the swing level of output signal is reduced then the dynamic power component is also reduced. If the swing level of signal V_{DD}, at output node is reduced then the power from first component in (1) is reduced by a ratio of $\left(\frac{V_{sig}}{V_{DD}}\right)\times 100$ %. A new 12 transistor adder is proposed with twisted diode connection transistors. The proposed 12T adder reduced the power consumption and power-delay product (PDP) considerably compare to 10T adder.

II. ADDER DESIGN

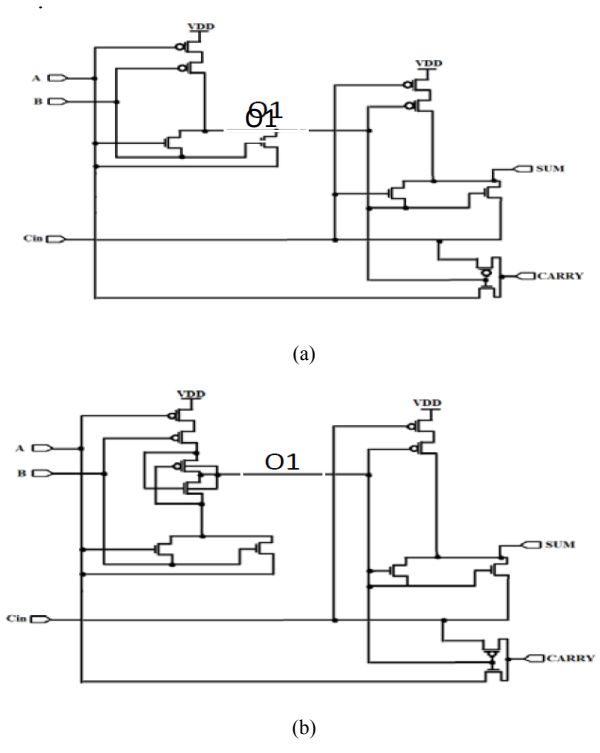


Figure 1 SERF Full Adder (b): Proposed 12T Full Adder

In [1] 10T SERF (Static Energy Recovery Full) adder circuit shown in Fig 1(a) is given. In the current work, a 12T adder is proposed with modification to 10T SERF adder as shown in Fig 1(b). A twisted diode connected coupler consisting of Pmos (Po1) and Nmos (No1) is inserted at node 'O1'. Assume that A='0' and B='0' initially. P1 and P2 are turned ON. Node Y starts charging to VDD. Assume that node X is at logic '0'. Thus, Po1 is ON. Output O1 starts charging to VDD. As Y charges above VT, No1 is turned on. Since output O1 is at VDD, it attempts to turn off Po1 by substrate biasing. High value at node X causes Po1 to turn off. Thus O1 level degrades to a value lower than VDD because of charge sharing between node X and O1

The Voltage level at O1 is given by Eq. (2) and (3).

$$V_{out\_H} = V_y(1 - e^{-t_{chg} / R_{MP2}.C_{load}}) \quad (2)$$

$$V_{out\_L} = V_x.e^{-t_{dchg} / R_{MN2}.C_{load}}) \quad (3)$$

Where,

$$R_{MP} = \frac{1}{\mu_p C_{OX}\left(\frac{W_{MP}}{L}\right)(V_{SG} - |V_{THP}|)} \quad (4)$$

$$R_{MN} = \frac{1}{\mu_n C_{OX}\left(\frac{W_{MN}}{L}\right)(V_{GS} - V_{THN})} \quad (5)$$

A lower output level helps to reduce the power as given by Eq. (1) and Eq. (2).

III. ANALYSIS AND SIMULATIONS

The simulation results of 10T and 12T adder for power analysis are given in Table I and plotted in Fig. 2. The comparison graph shows a sharp reduction in12T adder power compared to 10T adder. For a voltage range of 0.6V to 1.4V percentage of power reduction varies from 86.3% to 58.4% respectively. This validates the power reduction technique based on twisted diode connection transistors.

TABLE I. POWER ANALYSIS AND COMPARISON OF 10T AND 12T ADDER IN µW

VDD (Volt)	10T	12T
0.6	0.0291	0.004
0.7	0.745	0.015
0.8	4.407	0.078
0.9	11.269	0.422
1	21.125	1.894
1.1	34.282	6.118
1.2	51.639	14.354
1.3	74.215	26.916
1.4	102.187	43.803

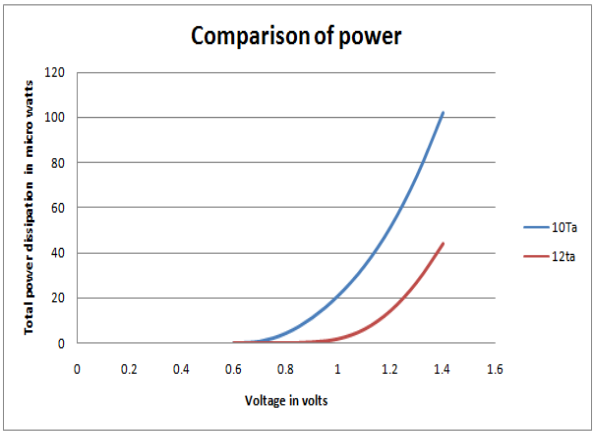
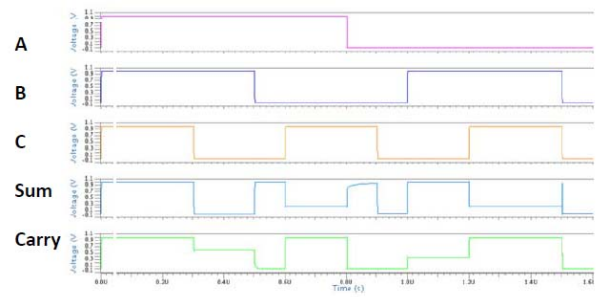
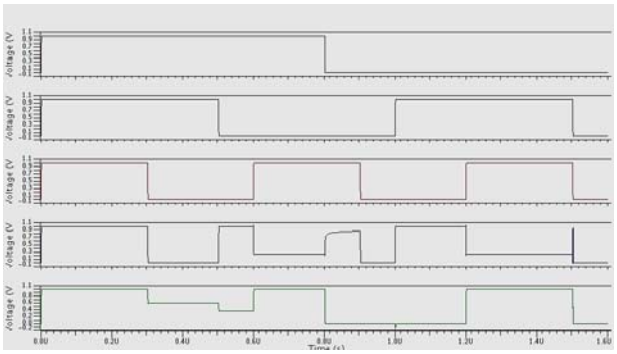


Figure 2 Power Comparison of 10T and 12T Full Adder

The simulated waveforms that verify the Adder characteristics are given in Fig.3 for completeness. As can be seen from the waveforms, full swing is not utilized because NMOS transistors will transmit VDD-VT for input VDD and PMOS will transmit |VTp|. Substrate bias effect will further reduce the output swing as explained in the previous section.



(a)



(b)

Figure 3 (a) Sum Output, (b) Carry Output

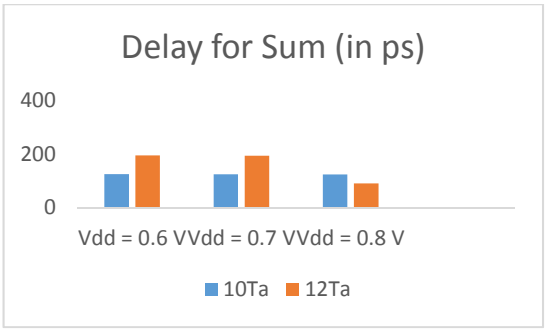
Since, the design has been tested on the low power node, sample delay simulations have been performed for VDD 0.6V, 0.7V and 0.8V for both Sum and Carry with respect to Cin. As is expected in the Full Adder circuit, Cin to Sum is the critical path. The result of delay in ps is listed in Table VI.

TABLE II. DELAY IN SUM AT DIFFERENT VDD

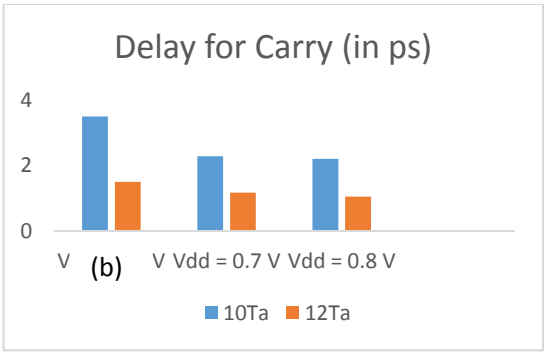
VDD	Delay (in ps) for 10Ta	Delay (in ps) for 12Ta
0.6	124.47	194.35
0.7	123.83	193.07
0.8	123.26	89.573

TABLE III. DELAY IN CARRY AT DIFFERENT VDD

VDD	Delay (in ps) for 10Ta	Delay (in ps) for 12Ta
0.6	3.5036	1.4980
0.7	2.2850	1.1658
0.8	2.2030	1.0480



(a)



(b)

Figure 4 (a) Delay for Sum, (b) Delay for Carry

Figure 5

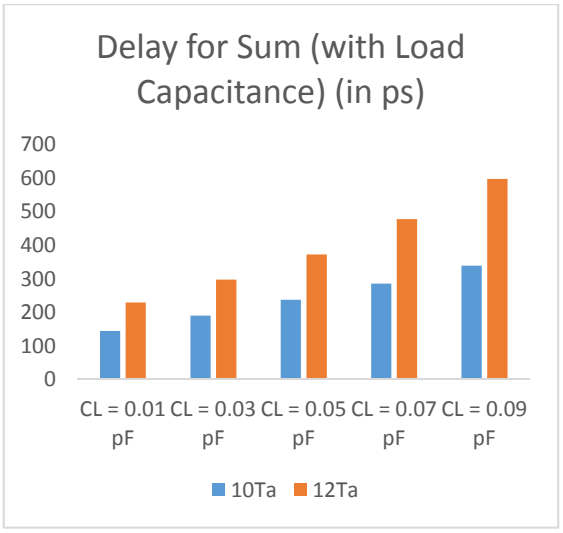
Furthermore, analysis for delay with changing Capacitive Load has been performed up to both Sum and Carry. As is expected delay increases with increasing Capacitive load for both 10T and 12T adders.

TABLE IV. DELAY IN SUM AT DIFFERENT CAPACITIVE LOAD

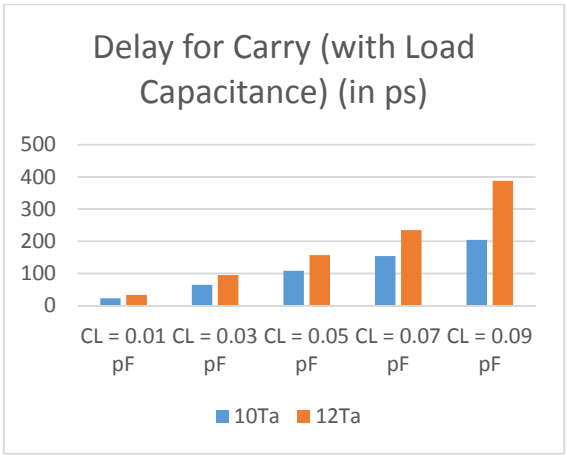
C_L	Delay (in ps) for 10Ta	Delay (in ps) for 12Ta
0.01 P	144.45	229.05
0.03 P	190.19	297.65
0.05 P	237.70	372.88
0.07 P	286.14	478.10
0.09 P	339.44	597.87

TABLE V. DELAY IN CARRY AT DIFFERENT CAPACITIVE LOAD

C_L	Delay (in ps) for 10Ta	Delay (in ps) for 12Ta
0.01 P	22.593	33.232
0.03 P	64.586	94.901
0.05 P	107.89	156.82
0.07 P	153.88	234.41
0.09 P	204.19	387.82



(a)

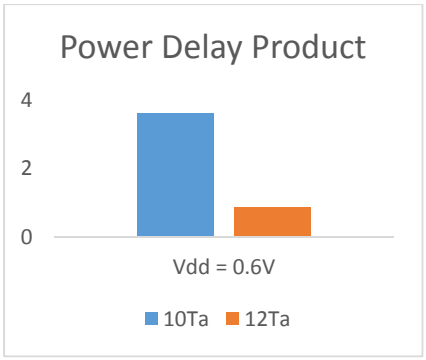


(b)

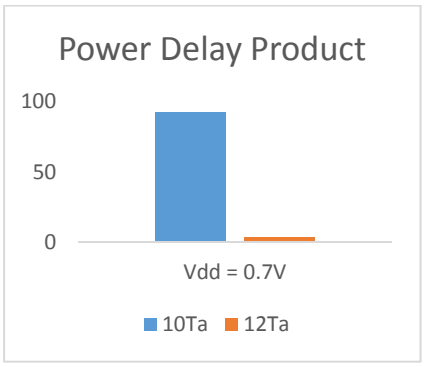
Figure 6 (a) Delay for Sum versus Capacitive Load, (b) Delay for Carry versus Capacitive Load

TABLE VI. COMPARISON OF POWER DELAY PRODUCT (PDP) FOR DIFFERENT V_{DD}

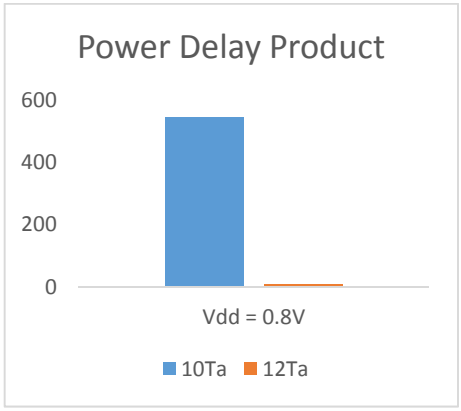
V_{dd}	Power in µW for 10Ta	Delay (in ps) for 10Ta	Power Delay Product (µWps)	Power in µW for 12Ta	Delay (in ps) for 12Ta	Power Delay Product (µWps)
0.6 V	0.0291	124.47	3.62	0.0044	194.35	0.855
0.7 V	0.745	123.83	92.25	0.0152	193.07	2.93
0.8 V	4.407	123.26	543.20	0.0780	89.573	6.98



(a)



(b)



(c)

Figure 7 Comparison of PDP of 10T and 12T adders at (a) 0.6V (b) 0.7V and (c) 0.8V

As can be seen from Table VI, a comparison of Power Delay Product for 0.6V, 0.7V and 0.8 V is given. There is 76.38% reduction in PDP at 0.6V, 97.63% reduction in PDP at 0.7V and 98.72% reduction in PDP at 0.8V.

IV. CONCLUSION

In this paper, an efficient method for reduction of power in adder circuit has been given. Although the number of transistors is increased, the power consumption of proposed 12T adder and Power Delay product are reduced substantially. Twisted diode connected coupler provides power reduction as the threshold voltage decreases which further helps in decreasing voltage swing at output node.

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