Analysis of SRAM Bit Cell Topologies in Submicron CMOS Technology

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***Abstract* - The paper investigates on the design aspects of different SRAM cells for access time, power consumption and static noise margin. All the designs are made by using standard 90nm CMOS process. Simulations have been done for 6T, 7T, 9T and 10T SRAM cells. 10T SRAM cell shows the best SNM among all the simulated cells. 9T shows least power and least access time. 6T cells stability limits the potential power saving achievable by voltage scaling while proposed 9T cells enhance stability. Layouts are also being made to create as compact a cell as possible. The results are compared with the actual known results and have been found justified.**

Keywords - SRAM cell, cell ratio, pull up ratio

I. INTRODUCTION

SRAM [1-4] is commonly used as on- chip cache memory and fabricated using the same technology as the other logic circuits. It is preferred over the other types of memories due to small access time, relatively small area, no charge refresh required and negligible static power dissipation [5-8]. The 6T cell is widely accepted and has become synonymous with SRAM. The conventional 6T cell brings to light several shortcomings when analyzed for performance in deep submicron and sub 1V supply processor design. With shrinking device size and exponential increase in the static power consumption necessity of the day is to explore alternative advanced cell structures [9-13].

A singled ended 6T SRAM cell was designed for low voltage applications [1], a 7T SRAM cell was used to design a low power cache memory [7], 8T SRAM was tested for variability tolerance and low votage operation [9] and 10T and 11T SRAM [14-15] were tested for low voltage at lower technology nodes for different applications. It was found that there is a need to discuss the requirement for different SRAM architectures for different architectures.

In this paper we have designed all the above mentioned SRAM architecture in submicron technology and analyzed their performance for varied applications. we have followed modular approach as there are various subsystem that constitute a total SRAM. RAM designing follows modular approaches there are various subsystems that constitute a total SRAM. These include simulation and calculation of the parameters of 6T SRAM cell, 7T SRAM cell, 9T SRAM cell and 10T SRAM cell and finally comparing all their parameters. The aspect ratios of each transistor are appropriately chosen for 90nm CMOS technology to obtain the desired results. Also, the other parameters in designing SRAM such as cell ratio are taken into consideration. All cells are simulated using TANNER EDA software, layout in Microwind and calculated SNM using MATLAB software. The results are compared with the actual known results and have been found justified.

II. CIRCUIT DESIGN AND ANALYSIS

The SRAM design consisted of sizing the transistor and determining the read and write stability. The layout was performed to create as compact a cell as possible.

The conventional 6T SRAM bit cell as shown in Figure 1, consist of two cross coupled inverters and two pass transistors are connected to complimentary bit lines. The transistors NMOS_2 and NMOS_3, known as access transistors are connected to wordline for writing data into the bit cell from bitline. The bitline (BL) carry data to the sense amplifier from the bit cell. Read, Write and Hold data are the three main operations of the SRAM cell. The main performance parameter for Read and Hold is the static noise margin. During Read operation the wordline is "HIGH" and the bitline is precharged to "HIGH".

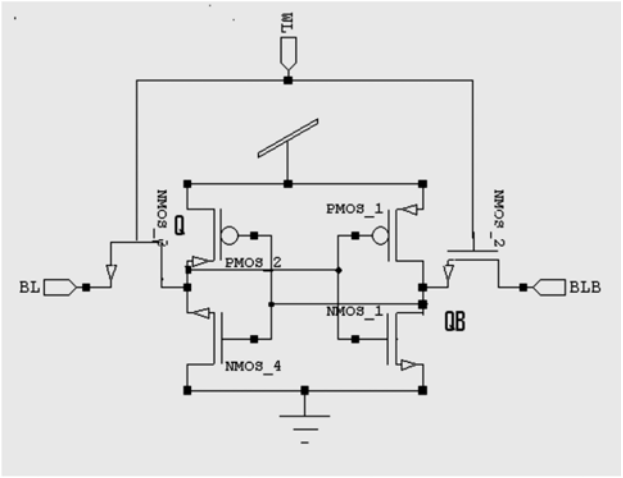

Figure 1: 6T SRAM cell

The access transistors (NMOS_2 and NMOS_3) disconnect the cell from the bitlines, if the word line is not asserted. The cross coupled inverters reinforce each other since they are connected to the power supply.

Three main operations of SRAM are: write, read and hold. During memory read, the bit-lines that are already precharged to logic 1 are connected to the cell nodes through the access transistors. The cell node that stores logic 0 is momentarily pulled-up using the access transistor which adversely affects SNM. The cell should remain stable during read and write operations.

On switching the word line to off state the access devices turn off, disconnecting the cell nodes from the bit-lines the cell is now in the retention state. The two CMOS inverters will reinforce the previous stored value in the cell due to positive feedback. Highly capacitive bit-lines are precharged to the logic 1 before initiating cell read operation. During cell read, the bit-line connected to the cell node that stores a logic 0 is discharged somewhat using the access transistors. Whereas the bit-line connected to the node of the cell storing logic 1 remains unaffected. There is a small difference in bit-line voltage developed due to this which is in turn read using the sense amplifier and converted to appropriate logic level voltages. In the retention state the load device connected to the node storing 1 and the driver connected to the node storing logic 0 are conduct in their linear or triode region of operation.

During cell read operation the access transistors connect the cell nodes q and q-bar to the precharged bit lines. The voltage at the node q-bar, that stores logic 1 remains unchanged whereas the voltage at bit-line that is connected to the node q which stores logic 0 is discharges by a small amount. This causes small difference in the voltage levels of the bit-lines which is sensed and amplified by the sense amplifier and converted to the full logic swing.

Voltage of the node q during read operation rises a little above 0V level since it is connected to the precharged bit-line which could in turn cause NMOS_1 to start conducting and bring down the voltage at node q-bar. To prevent this potential flip the state of the cell the conductivity of NMOS_1 and NMOS 3 should be sized properly.

Since the bit-line capacitance is large as compared to the cell node capacitance thus voltage swing during read operation is small.

Appropriate sense amplifier with proper response characteristics can be connected to the bit-lines to convert bit-line voltage swing to logic voltage output. Appropriate I_{cell} can set by transistor sizing to meet the desired voltage swing ΔV and timing requirements $\Delta\tau$ over the bit-lines.

During write operation, due to the high capacitance of the bit-lines they are first set to appropriate voltage level the and then word-line is enabled to select the cell. The Access devices NMOS_2 and NMOS_3 should have sufficient conductivity to bring down the voltage at cell node q below the threshold voltage of the pull-up device PMOS_1 to make it conduct in saturation region since its drain terminal is connected to node q-bar which is at logic 0. Cell sizing is appropriately to bring down the voltage at node q-bar to logic 1 and force NMOS_1 to conduct and bring down the voltage at node q and turning NMOS_1 off, thus flipping of the cell state.

The 7T cell shown in Figure 2 is designed to overcome the disadvantages of static noise margins at low VDD. NMOS pass transistor NMOS_5 can be used to open or close the feedback loop that connects the two inverters. Separate data path is used to read the cell during logic 0 and logic being stored at the cell node q. For logic 0 being stored : During read operation the node that stores logic 0 is pulled up due to formation of voltage divider with the driver of the complementary inverter. This is prevented by switching the NMOS_5 pass transistor off and with the precharged bit-line is prevented.

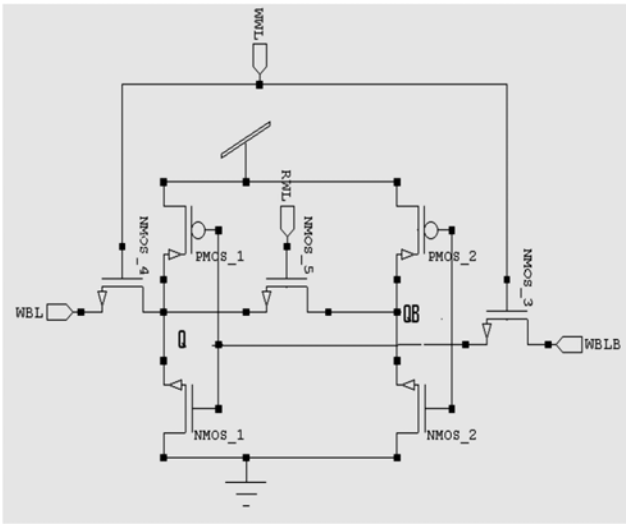

Figure 2: Schematic of 7T SRAM cell

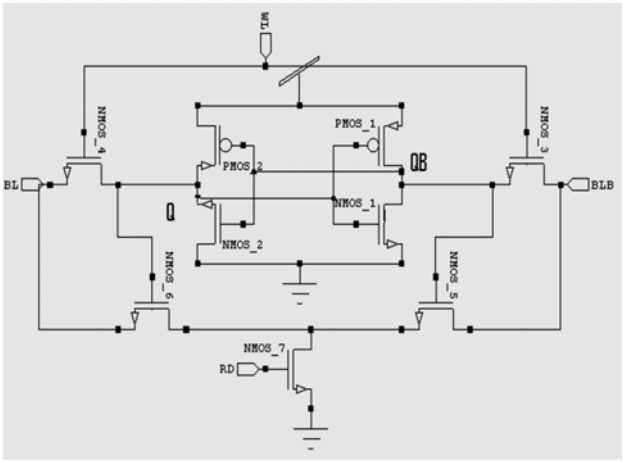

Figure 3: Schematic of 7T SRAM cell

The 9T SRAM cell is shown in Figure 3 and 10T SRAM cell is shown in Figure 4.

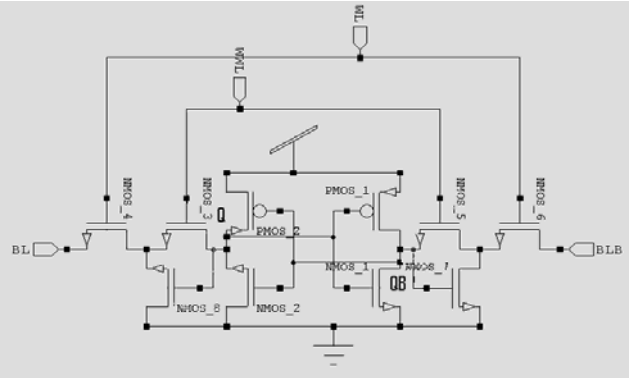

Figure 4: Schematic of 10T SRAM cell

III. RESULT AND DISCUSSION:

All the four types of SRAM cells discussed above are implemented in TANNER tool using 90nm CMOS technology. Layout analysis was performed using Microwind and waveform corresponding to write operations was plotted. Measurements were done for access time and power consumption. Voltage transfer characteristics and static noise margin of the cell was calculated.

Figure 5 (a) – (d) shows the waveforms of write enable (WE) node corresponding to a given pulse train repeated periodically for a 6T, 7T, 9T and 10T.

In Figure 5(a) waveform of WE is the pulse train of 010000 bits repeating periodically is being plotted. The write operation is performed when WE node is at high potential. During the first bit of WE when WE node is at ground potential then ND is at high potential but when WE goes to high potential then the input data given by Voltage source VIN which is 0 is written on to the cell, similarly VINB which is 1 is written on the other half of the cell. Now WE node again goes to ground potential, then the cell retains its value until WE node goes to high potential again. Voltage at NA node is complement to NB node as both these nodes are present at opposite ends of cross coupled inverters. BIT and BITB are the nodes which are present after the access transistors and are complementary in nature. As they are present after the access transistors therefore their waveform is coming out to be a little distorted and there is a small drop due to leakage parameters of access transistors.

In Figure 5(b) waveform of WWL is the pulse train of 010000 bits repeating periodically.The write operation is performed when WWL node is at high potential. During the first bit of WWL when WWL node is at ground potential then NC is at high potential but when WWL goes to high potential then the input data given by voltage source VIN which is 0 is written on to the cell.Now WWL node again goes to ground potential, then the cell retains its value until WWL node goes to high potential. Voltage at NA node is complement to NC node as both these nodes are present at opposite ends of cross coupled inverters. In Figure 5(c) waveform of Waveform of RWL is the pulse train of 010000 bits repeating periodically as usual. The write operation is performed when RWL node is at high potential. During the first bit of RWL when RWL node is at ground potential then NB is at high potential but when RWL goes to high potential then the input data given by Voltage source VIN which is 0 is written on to the cell. Now RWL node again goes to Ground potential, then the cell retains its value until WE node goes to high potential. Voltage at NA node is complement to NB node as both these nodes are present at opposite ends of cross coupled inverters. BL and BLB are the nodes which are present after the access transistors and are complementary in nature.

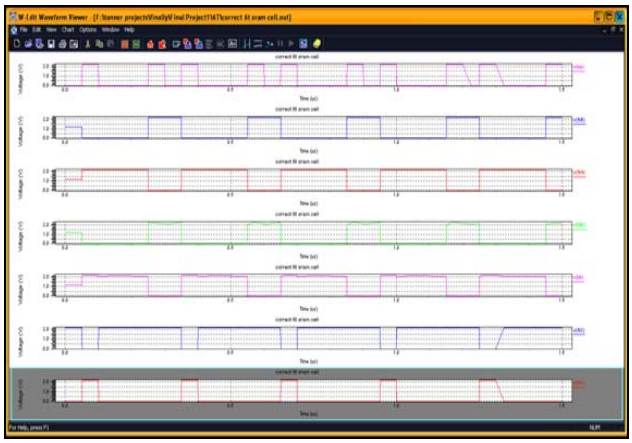

Figure 5-a. Waveform of WE for 6T

Figure 5-b. Waveform at WE for 7T

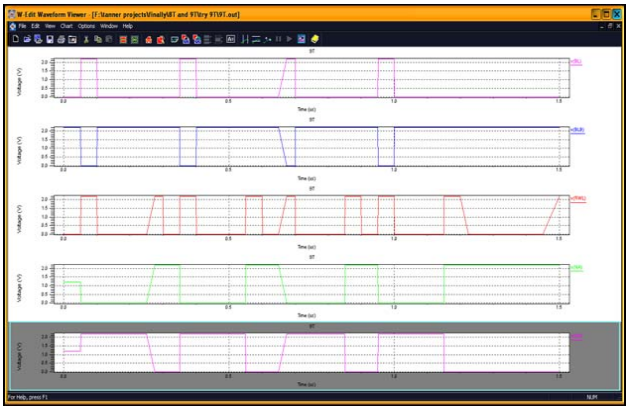

Figure 5-c. Waveform at RWL for 9T

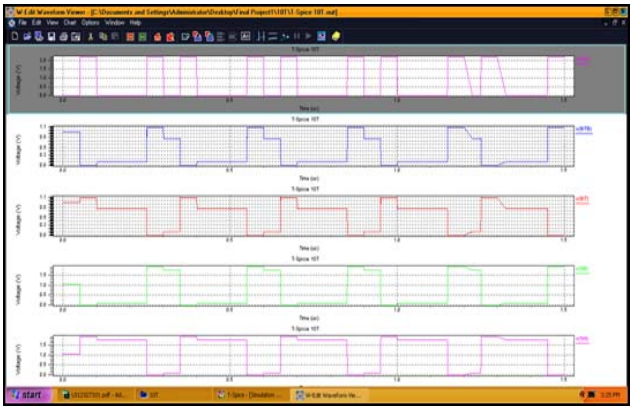

Figure 5–d. Waveform at RWL for 10T

In Figure 5(d) waveform of WE is the pulse train of 010000 bits repeating periodically. The write operation is performed when WE node is at high potential. During the first bit of WE when WE node is at ground potential then NB is at high potential but when WE goes to high potential then the input data given by Voltage source VIN which is 0 is written on to the cell. Now WE node again goes to Ground potential, then the cell retains its value until WE node goes to high potential. Voltage at NA node is complement to NB node as both these nodes are present at opposite ends of cross coupled inverters. BIT and BITB are the nodes which are present after the access transistors and are complementary in nature. As they are present after the access transistors therefore their waveform is coming out to be a little distorted

Figure 6(a) – (d) shows the voltage transfer characteristics of all the four topologies.

Figure 6(a)

Figure 6(b)

Figure 6(c)

Figure 6(d)

Figure 6: Voltage transfer characteristics of different bit cell topologies

In figure 6(a) VTC of 6T SRAM cell prepared in T-SPICE. As it can be seen that the curve starts from 1.7V instead of 2.2V, this is due to the voltage drop in the pull up transistors. When the VIN voltage is between -5.0000e-001 to 5.9746e-001, the VOUT voltage is at high voltage. When the VIN voltage is between 7.5424e-001and 1.5381e+000, the VOUT voltage is in transition. When the VIN voltage is between 1.6949e+000and 2.1653e+000, the VOUT voltage is at low potential. This VTC is used to obtain the butterfly structure and calculate SNM of the cell.

In figure 6(b) the VTC of 7T SRAM cell. There is full voltage swing in this case from 2.2V.When the VIN voltage is between 0.0000e+000 to 7.2850e-001, the VOUT voltage is at high voltage. When the VIN voltage is between 7.5200e-001 and 1.5381e+000, the VOUT voltage is in transition. When the VIN voltage is between 1.0575e+000 and 2.1855e+000, the VOUT voltage is at low potential.

Figure 6(c) shows the VTC of 9T SRAM cell. When the VIN voltage is between 0 to 6.0000e-001, the VOUT voltage is at high voltage. When the VIN voltage is between 9.0000e-001 and 1.500e+000, the VOUT voltage is in transition.When the VIN voltage is between 1.8000e+000 and 2.1000e+00, the VOUT voltage is at low potential.

In Figure 6(d) VTC of 10T SRAM cell is shown. As it can be seen that the curve starts from 2.0V instead of 2.2V, this is due to the voltage drop in the pull up transistors. When the VIN voltage is between 0 to 7.4100e-001, the VOUT voltage is at high voltage.When the VIN voltage is between 8.6450e-001 and 1.1115e+000, the VOUT voltage is in transition. When the VIN voltage is between 1.2350e+000 and 2.0995e+000, the VOUT voltage is at low potential.

The transfer characteristics of both the inverters in the SRAM cell can be plotted which is known as butterfly curve. SNM of the cell can then be obtained from it. Figure 7(a) – (d) show the butterfly curve of the four SRAM topologies.

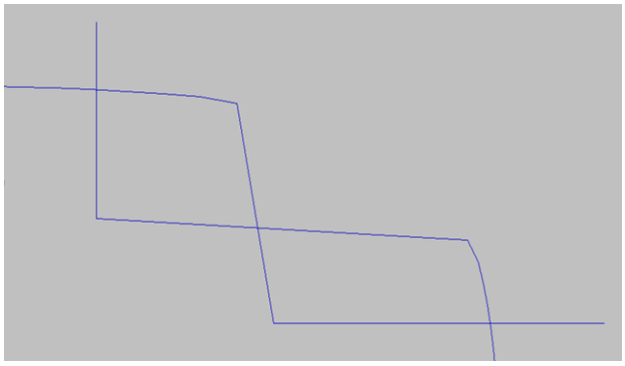

Figure 7(a) 6T

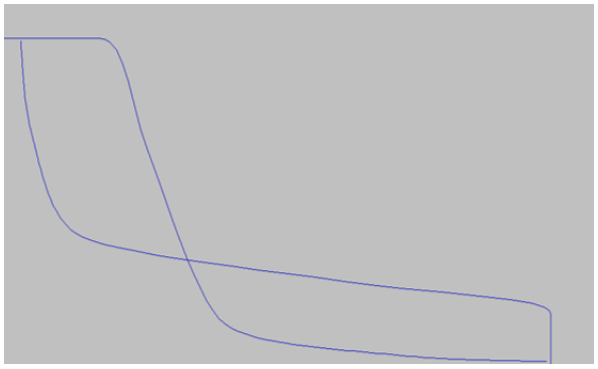

Figure 7(b) 7T

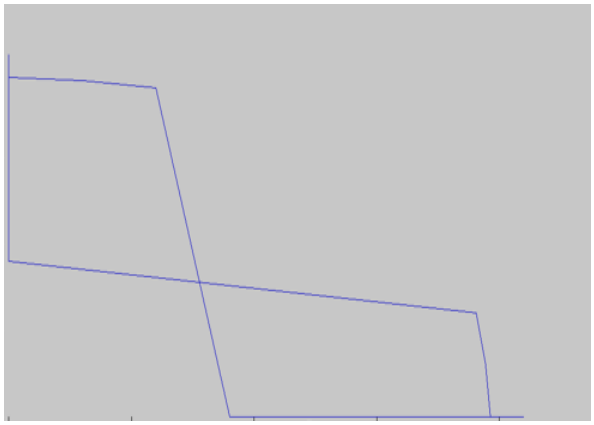

Figure 7(c) 9T

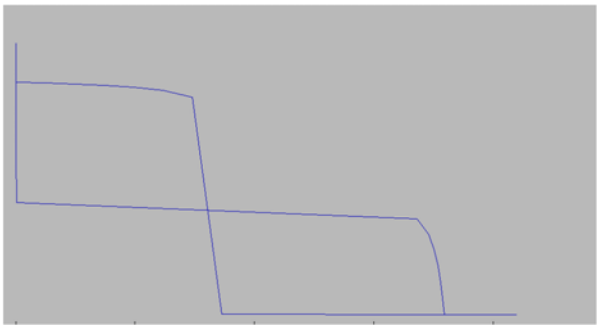

Figure 7(d) 10T

Figure 7: Butterfly curve of all the bit cell topologies.

The value obtained for SNM of a 6T SRAM cell is 1.01. Figure 7(b) is the butterfly diagram of 7T SRAM cell prepared in MATLAB. The SNM obtained is 1.10. Similarly for 9T and 10T SRAM cell the SNM obtained is 1.17 and 1.19 respectively.

Finally the layout is performed for all the SRAM cells as shown in Figure 8(a) – (d).

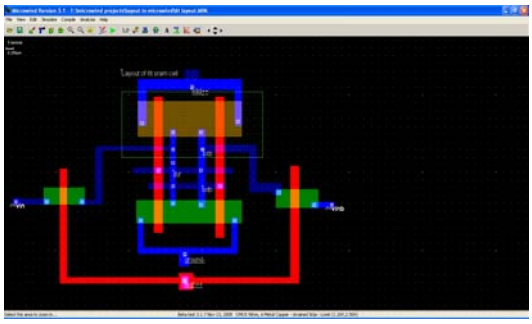

Figure 8(a) 6T

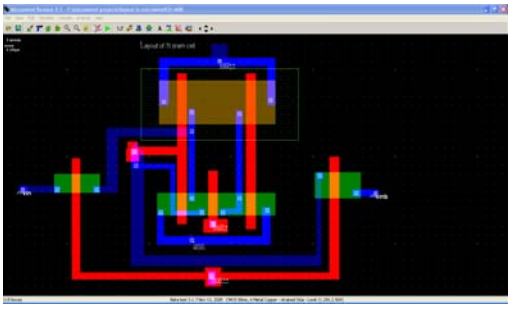

Figure 8(b) 7T

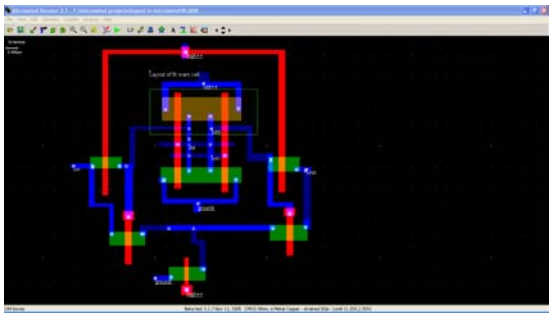

Figure 8(c) 9T

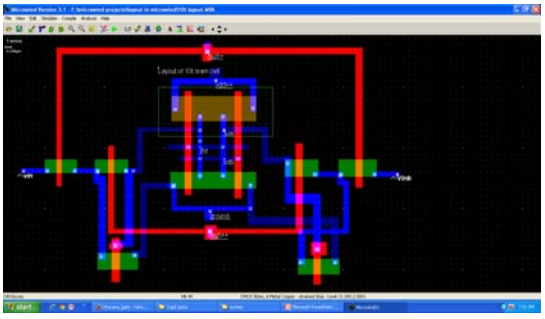

Figure 8(d)

The measured results of access time corresponding to 6T, 7T, 9T and 10T is compared in Table I.

TABLE I. MEASURED RESULTS

Cell type	6T	7T	9T	10T
Access Rise Time	7.0002e-007	1.4973 e-006	1.9255 e-007	7.0001 e-007
Trigger Time	1.5174e-006	2.5064 e-006	8.5050 e-007	1.5119 e-006
Target Time	8.1735e-007	1.0091 e-006	6.5796 e-007	8.1192 e-007
Access Fall Time	9.9999 e-007	1.9965 e-006	5.9955 e-007	9.9989 e-007
Trigger Time	2.0174 e-006	3.5063 e-006	1.1505 e-006	2.0118 e-006
Target Time	1.0174 e-006	1.5098 e-006	5.5096 e-007	1.0120 e-006

Access time increases for 7T cell in comparison to 6T cell due to the fact that the width of access transistors used for 7T cell is large and hence have large W/L ratio and thus increasing parasitic capacitance. However W/L ratio of 9T cell is taken smaller than 7T cell and hence it has less parasitic capacitance and thereby less access time. Similarly 10T cell has large W/L ratio and therefore has large access time in comparison to 9T cell. Figure 9 compares SNM of various SRAM cells.

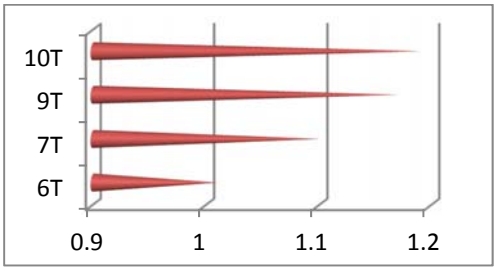

Figure 9: Comparison of SNMs of 6T, 7T, 9T and 10T SRAM cells

SNM increases as we move from 6T to 10T cell which suggest that 10T is most stable among all the simulated cells.

TABLE II: COMPARATIVE RESULTS

CELL	AVERAGE POWER	MAXIMUM POWER	MINIMUM POWER
6T	6.175318 e-004 watts	7.137491 e-004 watts	5.712297 e-004 watts
7T	2.274558 e-004 watts	2.330134 e-004 watts	1.475349 e-004 watts
9T	1.4973 e-006 watts	3.339977 e-004 watts	2.396597 e-008 watts
10T	3.239679 e-004 watts	5.136656 e-004 watts	1.911629 e-004 watts

As the read stability and writability of 6T SRAM cell is limited in subthreshold region, therefore it difficult to operate it in this region. Therefore other cells have been

explored. The 7T SRAM cell uses single bitline for read and write operation while 9t SRAM cell uses different set of transistors for read and write operation, therefore their power dissipation is less as compared to 6T cell. Table II compares the power dissipation for various SRAM cells.

IV. CONCLUSION

As SRAM continues to dominate the total area and power consumption in modern SoC, subthreshold SRAM provides an effective strategy for total power saving. Stability issue, being the key concern in subthreshold designs, must be considered seriously. For low-leakage and high-speed circuits concern should be on the factors SNM, power consumption and access time. This project tries to find out the solution for SRAM memory cells in all the above aspects. 10T SRAM cell shows the best SNM among all the simulated cells. 9T shows least power and least access time. 6T cells stability limits the potential power saving achievable by voltage scaling. While proposed 9T cells enhance stability

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