Low Power Balun-LNA for Subsampling Architecture of Receiver

Fanzhen Meng¹,², Hong Liu¹, Mingliang Wang¹, Tong Tian¹,²*

¹Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai, China
²University of Chinese Academy of Sciences, Beijing, China

Abstract — A single-ended-to-differential conversion balun-LNA is proposed in this paper for subsampling architecture of receiver. The LNA adopts the inductively degenerated common-source common-gate (cascade) structure with noise canceling technique, which can achieve high gain and low noise figure without extra components and power consumption. For the subsampling receiver of IoT narrowband application, the LNA is integrated in 65 nm CMOS. It can achieve a noise figure of 1.5dB at the 780MHz, a differential voltage gain of 30 dB and gain and phase mismatch within 0.5 dB and 5° in the range from 775MHz to 785MHz, which is adequate for most of IoT applications. The proposed LNA consumes about 1.6mA with 1.2 V voltage supply.

Keywords - Subsampling receiver; Balun-LNA; 780MHz IoT; low power

I. INTRODUCTION

With the increasing requirements for wireless communication of Internet of Things, we pay more attention on the performance, such as high integration, low power, low cost and multi-mode [1,2,3]. In order to meet the above performance, low power subsampling architecture of receiver should be used [4]. Low-noise amplifier (LNA) as the first block in the receiving chain is of great importance. Its voltage gain, noise figure and power consumption can affect the performance of the whole system [5,6,7].

Usually, the common-source common-gate (cascode) structure could be widely used for LNA design [8,9,10]. Common-gate (CG) topology can easily eliminate miller effect and common-source (CS) can acquire high voltage gain. For example, the inductively degenerated cascode configured LNA exhibits high gain and low noise figure, as shown (Fig. 1 (a)) [11]. In order to restrain the common mode noise and reduce parasitic couplings, the single-ended LNA should be converted to differential output. Generally, the off-chip baluns could be used to achieve differential signal. Although the off-chip baluns decrease the complexity of the system and the performance is better, it sacrifices the size and integration level. Fortunately, the noise-cancelling differential configuration LNA has been reported as shown (Fig. 1 (b)) [12,13,14]. For example, an inductorless low-noise amplifier (LNA) with the active balun can achieve with 15 dB gain and NF of 3.5 dB with gain and phase errors below 0.3 dB and 2 degrees [14].

Fig.1(a) Schematic of the Inductively Degenerated Cascode Configured LNA and (b) the Noise-Cancelling Differential Configuration LNA
Although the CG-CS differential structure can achieve high voltage gain and generate the differential signal of phase opposite and equal amplitude, which is very sensible to the process variation [13]. Considering the advantages of the inductively degenerated cascode and the noise-cancelling differential configuration, new balun-LNA is reported in [11,15]. The balun-LNA consumes only 2 mA current from a 1.8 V supply and exhibits a differential voltage gain of 30.4 dB and a noise figure of 1.8 dB [15]. However, large inductor L increases size of the chip. Otherwise, lower supply voltage of MOS transistor with the new CMOS process technology, such as in the weak inversion (WI) or moderate inversion (MI) region, can make power consumption further reduced [16,17], such as in the MI–WI region, the power consumption of the LNA is only 0.68mW [17].

In the paper, the inductively degenerated balun-LNA with the noise canceling technique is proposed in Section II. Architecture and analysis of the balun-LNA are introduced in Section III. Circuits design and the performance of the balun-LNA will be exhibited in Section IV. Finally, the conclusions and discussion are drawn in Section V.

II. ARCHITECTURE AND ANALYSIS OF PROPOSED LNA

A. Architecture of LNA

The proposed balun-LNA is shown (Fig. 2), based on inductively degenerated cascode differential configuration. The RF signal coming from antenna is amplified by LNA. Firstly, transistors M1 and M2 consisting of the cascode topology could achieve high gain and input impeding matching, with the inductors Ls, Lg and capacitor Cg. And then transistors M3 and M4 consisting of the common-gate and common-source differential topology can provide the noise canceling and distortion canceling. The single-ended RF signal is transferred from the drain of M2 to the source of M3 and the gate of M4 through the capacitor Cc for differential output. Capacitor Cb provides the AC coupling to ground and bias supply voltage makes enough current differential output, which avoids using the larger inductor L coupling to DC current. The sizes of M3 and M4 should meet the proper proportion for acquiring the signal of equal amplitude and opposite phase. In addition, the larger resistor RCG and RCS could be used to achieve high voltage gain.

Fig.2 Schematic of the Proposed Balun-LNA

B. Input Matching

The input impedance matching of the balun-LNA can easily achieve with the inductively degenerated inductors Ls, input impedance of Zin can be expressed as [9],

$$Z_{in} = j\omega (L_s + L_g) + \frac{1}{j\omega (C_{gs} + C_g)} + \frac{g_{m1} L_g}{(C_{p} + C_g)}$$

(1)

where $g_{m1}$ is the trans-conductance of M1 and $C_{gs}$ is the gate-source capacitance. From (1), the source degenerative inductor Ls can easily achieve the real matching without generating extra noises, and capacitor Cg could relax the constraint of power consumption. When input impedance of $Z_{in}$ is matched to 50Ω, thus: $\Re\{Z_{in}\} = 50 \Omega$ and $\Im\{Z_{in}\} = 0$.

The resonance frequency $\omega$ can be expressed as,

$$\omega = \sqrt{(L_g + L_s) (C_{p} + C_g)}$$

(2)

C. Noise Analysis

In order to analyze the noise figure of the balun-LNA in detail, noise figure of every stage would be listed respectively. Firstly, regardless of the noise contribution from the cascade stage M2, the noise figure NF1 of M1 can be calculated as [10, 18],

$$NF1 = 1 + \frac{\gamma + \delta}{2} \frac{\gamma + \delta}{\gamma + \delta + 1}$$

(3)

where $\gamma$, $\delta$, $\delta$ are process parameter. NF1 is determined by the trans-conductance $g_{m1}$ of M1 and the gate-source capacitance $C_{gs1}$ and capacitance $C_g$.

Secondly, the typical CG–CS topology is widely used, which has been analyzed in detail [14]. The noise figure NF2 of the CG–CS topology can be calculated as,
\[NF_2 = 1 + \frac{\gamma g_{m,CG} \left( R_{CG} - R_S \frac{1}{g_{m,CS}} R_C \right)^2}{R_S A_{v,2}^2} + \frac{\gamma g_{m,CS} R_C^2 (1 + \frac{1}{g_{m,CG}}) R_S}{R_S A_{v,2}^2} + \frac{(R_{CG} + R_C) (1 + g_{m,CG}) R_S}{R_S A_{v,2}^2}\]

(4)

where the second part and the third part are respectively the noise contribution from the CG transistor M3 and CS transistor M4, and the last part from the load. The voltage gain \(A_{v,2}\) of differential configuration can be expressed as [13],

\[A_{v,2} = g_{m,CG} R_{CG} + g_{m,CS} R_C\]

(5)

where \(g_{m,CG}\) is the trans-conductance of M3, \(g_{m,CS}\) is the trans-conductance of M4, \(R_{CG}\) and \(R_C\) are respectively the load resistance from M3 and M4, and \(R_S\) is output resistance of M2.

The noise figure \(NF_2\) of the CG–CS topology would be further analyzed by simulation, assuming that the trans-conductance \(g_{m,CS}\) is \(n\) times bigger than the trans-conductance \(g_{m,CG}\) and the load resistors \(R_{CG}\) is \(n\) times bigger than the load resistors \(R_C\). When CG transistor M3 is matched, \(R_S\) is the reciprocal of trans-conductance \(g_{m,CG}\) \((R_S = 1/g_{m,CG})\). Therefore, the noise figure and voltage gain of CG–CS topology can be respectively rewritten as (6) and (7),

\[NF_2 = 1 + \frac{4 \gamma g_{m,CG} R_{CG} R_S}{R_S A_{v,2}^2} + \frac{4 \left(1 + \frac{1}{n}\right) R_S}{R_S A_{v,2}^2}\]

(6)

\[A_{v,2} = 2 g_{m,CG} R_{CG}\]

(7)

From (6), \(NF_2\) is determined by the trans-conductance \(g_{m,CG}\) of M3 and the load resistors \(R_{CG}\). Because of the matching condition, the trans-conductance \(g_{m,CG}\) is 20mS and \(R_S\) is 50\(\Omega\). \(\gamma\) is about 4/3, and the load resistors \(R_{CG}\) is about 1000\(\Omega\) for high voltage gain. Noise figure \(NF_2\) of the CG–CS topology is clearly shown (Fig. 3), which noise figure \(NF_2\) would become smaller by increasing ratio \(n\) \((n = g_{m,CS}/g_{m,CG})\).

With impeding matching of CG transistor M3, the noise figure can’t be able to be reduced further. However, based on the inductively degenerated stage, the proposed balun-LNA achieves lower noise figure for the large \(R_S\) and small \(g_{m,CG}\).

According to the noise figure cascaded formula, the total noise figure of the balun-LNA can be expressed as [11],

\[NF = NF_1 + \frac{NF_2 - 1}{A_{v,1}}\]

(8)

Usually, the inductively degenerated cascade configuration has high voltage gain \(A_{v,1}\). Therefore, \(NF_1\) has an important effect on the total noise figure \(NF\) of LNA.

D. Gain and Phase Balance

The balun-LNA can provide the differential output signal, which is better suit for the following signal processing. Therefore, it is of great importance to make sure gain and phase balance of the CG–CS topology [13].
The schematic of the CG–CS topology with the parasitic effect is shown (Fig. 4). Capacitor $C_1$ is the total capacitor from M2, M3 and M4, and capacitor $C_{GS}$ and $C_{CS}$ is output capacitor [19]. The value of capacitor $C_1$ is written as

$$C_1 = C_{m2} + C_{m3} + C_{m4} (1 + g_{m3}(R_C)) + C_{m1} + C_{m4} (1 + g_{m4}(R_C))$$

(9)

The voltage gain of CG-transistor can be expressed as

$$V_{CG} = \frac{g_{mCG} R_{CG}}{1 + sR_{CG} C_G} + \frac{gm_{CS} R_{CS} + sR_{CS} C_S}{1 + sR_{CS} C_S}$$

(10)

The voltage gain of CS-transistor can be expressed as

$$V_{CS} = \frac{gm_{CS} R_{CS}}{1 + sR_{CS} C_S}$$

(11)

Operating at the low frequency, gain and phase balance of the CG–CS topology can be easily achieved [13, 20, 21]. Considering the signal transmission from $V_x$ to $V_{CG}$ and $V_{CS}$, the imbalance of the gain and phase can be calculated as

$$\Delta \phi = \phi_{CG} - \phi_{CS} - 180$$

$$= \tan^{-1} \left( \frac{R_{CG} C_G}{1 + g_{mCG} R_{CG} (1 + g_{mCS} R_{CS})} \right) - \tan^{-1} \left( \frac{R_{CS} C_S}{1 + g_{mCS} R_{CS}} \right)$$

(12)

$$\Delta V = 20 \log_{10} \left( \frac{V_{out,CG}}{V_{out,CS}} \right) = 20 \log_{10} \left( \frac{V_{in}}{R_{CG}} \right)$$

(13)

From (12) and (13), the reducing ratio $n$ ($n = g_{mCS} / g_{mCG}$) can further cancel the imbalance of the gain and phase. However, balance of the gain and phase would be affected for the high frequency fields.

F. Noise Canceling and Distortion

Considering the gain and phase balance, output signal of CG-transistor and CS-transistor should meet the equal gain and opposite phase [14]. And the output anti-phase voltage of CG-transistor can be calculated as

$$v_{noise,CG} = -i_{in} R_{CG}$$

(14)

Where $i_{in}$ is the input current noise, $R_{CG}$ is the output resistor of CG-transistor. The output voltage noise $v_{noise,CS}$ of CS-transistor is the same as $v_{noise,CG}$ of CG-transistor, thus:

$$v_{noise,CS} = -i_{in} R_{CS} = v_{noise,CG}$$

Therefore, the noise from the CG-transistor can be canceled.

With the nonlinearity of transistors, a controlled current source is modeled between drain and source. The output voltage difference of CG-transistor and CS-transistor can be written as,

$$\Delta v = v_{out,CG} - v_{out,CS} = V_{in} \frac{R_{CG}}{R_S}$$

(15)

Where $v_{in}$ is the input information signal, $R_S$ is the source resistor. Linearity of CG-transistor can be determined by $R_{CG}$. From (14) and (15), the nonlinear noise and distortion of CG-transistor can be canceled. Therefore, the linearity of the CG–CS topology can be determined by the CS-transistor.

III. CIRCUITS DESIGN AND SYSTEM PERFORMANCE

The proposed balun-LNA is design in 65nm CMOS technology. In order to achieve the differential signal of equal amplitude and opposite phase, gain and phase balance of the CG–CS topology is considered with the noise and distortion canceling. Generally, the imbalance of the gain and phase is within $\pm 0.5dB$ and $\pm 5^o$ in the signal bandwidth of most of IoT applications respectively. According to the above analysis, the ratio $n$ between trans-conductance $g_{mCS}$ and the trans-conductance $g_{mCG}$ is 4, which can achieve the lower noise figure NF. In addition, the lower supply voltage of the MOS transistor can reduce the power consumption of LNA.

A. S-parameters of Balun-LNA

Based on the inductively degenerated structure, balun-LNA could be used to generate the differential output signal with the high gain and low noise figure. Operating at the 780MHz, input matching and output matching inductors and capacitors is very large so that the off-chip matching is adopted. The circuit simulation shows that the S11 of LNA is about -20dB and the voltage gain of LNA is about 30dB at the 780MHz shown (Fig. 5 (a)).
By using the inequality between trans-conductance $g_m, CS$ and the trans-conductance $g_m, CG$, low noise figure can be achieved. The noise figure of the LNA spacing of 550MHz and 1GHz is shown (Fig. 5 (b)). The minimum NF is 1.5dB at the 780MHz.

**B. Gain and Phase Imbalance**

Further, the amplitude and phase imbalance of differential output signal remains within 0.5dB and 5 degrees in the signal bandwidth respectively as shown (Fig. 6 (a) and (b)). By adjusting to the bias of the CG-CS topology, gain and phase imbalance is reduced.

**C. Performance**

With the voltage supply of 1.2V, the current consumption of balun-LNA with noise-cancelling is 1.6mA. When the input RF frequency is 780MHz and input amplitude of signal is -90dBm, LNA can achieve better differential signal output at the data rate of 1Mbps. In addition, linearity of balun-LNA doesn’t need to be considered for the subsampling architecture. Compared to others, the performance of the proposed LNA is listed in Table I. The proposed LNA has advantages than others in terms of noise figure and power consumption. Owing to the balun-LNA with the noise cancelling technique, noise figure can be improved. And the power consumption can be reduced by the controlling the bias of transistors.
TABLE I. ESTIMATED PERFORMANCE COMPARISON

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption</td>
<td>6.75mW (1.5V)</td>
<td>2.88mW (1.2V)</td>
<td>21mW (1.2V)</td>
<td>3mW (1.2V)</td>
<td>3.6mW (1.8V)</td>
<td>1.92mW (1.2V)</td>
</tr>
<tr>
<td>Noise figure</td>
<td>- --dB</td>
<td>- -dB</td>
<td>- -dB</td>
<td>- -dB</td>
<td>- -dB</td>
<td>- -dB</td>
</tr>
<tr>
<td>Gain</td>
<td>15dB</td>
<td>16dB</td>
<td>13-15.6dB</td>
<td>7.6-16.6dB</td>
<td>30-34dB</td>
<td>30dB</td>
</tr>
<tr>
<td>Frequency</td>
<td>900MHz</td>
<td>900MHz</td>
<td>0.2-2GHz</td>
<td>0.2-2.0GHz</td>
<td>1.227GHz</td>
<td>780MHz</td>
</tr>
<tr>
<td>S11</td>
<td>- --dB</td>
<td>- -dB</td>
<td>- -dB</td>
<td>- -dB</td>
<td>- -dB</td>
<td>- -dB</td>
</tr>
<tr>
<td>Technology(CMOS)</td>
<td>0.18um</td>
<td>0.13um</td>
<td>65nm</td>
<td>0.13um</td>
<td>0.18um</td>
<td>65nm</td>
</tr>
</tbody>
</table>

*The total power consumption* *Unloaded voltage gain of balun-LNA core*

IV. CONCLUSIONS

The proposed balun-LNA for the subsampling architecture of receiver is analyzed in detail. The inductively degenerated cascade differential configuration achieves better matching, high gain and low noise figure. The inequality of trans-conductance \( g_{m,CG} \) and the trans-conductance \( g_{m,CG} \) provide lower noise figure. With noise canceling and distortion canceling, gain and phase balance of differential output signal are improved. The results show that the proposed balun-LNA has advantages in terms of noise figure and power consumption. Otherwise, linearity would be improved by highly linear-enhancement technique. Further, the advanced CMOS technologies reduce power dramatically and noise figure would be improved by Q-enhancement technique.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflicts of interest.

ACKNOWLEDGMENT

This work is supported by Shanghai Municipal Commission of Economy and Information under Grant (N1311-32), National Science and Technology Major Project, China (No.2011ZX0205-004).

REFERENCES


