Avalanche Characteristic of Vertical Impact Ionization MOSFET (IMOS) 
Equivalent Circuit Model

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Abstract — Snapback breakdown is the second order effect of avalanche breakdown in a device. Snapback occurs when the excess supply voltage and high currents created flow through the device and become unstable. These two breakdowns are used to explain the concept of Vertical Impact Ionization MOSFET (IMOS) in its Equivalent Circuit Model. The equivalent circuit model design consists of MOS transistors that represent the avalanche characteristic, while the Bipolar Junction Transistor represents the snapback characteristics with a generated-hole-dependent base resistance. The part models for parasitic bipolar or BJT is combined with a MOS transistor model to represent the both avalanche and snapback breakdown. The results show that 90% of the analysis of the subthreshold slope value of the circuit simulations is similar to the reference experimental value. Therefore, the equivalent circuit model can be used to represents the behavior of vertical IMOS in circuit environment in terms of simulations.

Keywords—Impact Ionization, Vertical IMOS, Planar IMOS, Equivalent Circuit Model, Snapback, Avalanche Characteristic

I. INTRODUCTION

Impact Ionization (II) MOSFET (IMOS) [1] have been proposed and studied to solve fundamental problems occur in MOSFET when the transistor continuously scaling down. The value of subthreshold slope is limited to 60mV/dec at room temperature [1]. It has been proven that IMOS can have a lower subthreshold slope than the Conventional MOSFET (CMOS) [2]. The performance of IMOS which is can have a lower subthreshold slope to make the continued scaling of CMOS technology possible.

Lateral IMOS works on the avalanche breakdown mechanism that occurs by II instead of diffusion of electrons to provide carrier [3]. This transistor is basically composed of p-i-n diode which is the main idea of this type of transistor which is applying a voltage between the source and drain near the breakdown voltage of the p-i-n diode [4]. The inversion layer formed under the gate makes a high horizontal electric field achieved, which inducing breakdown, the avalanche is then limited by the channel resistance [5].The lateral IMOS also had solved some problems faced by MOSFET before this. It includes the problems about short channel effects and gate leakage [6]. Although this new kind of transistor gives many advantages for transistor technology, there are some problems arose from this structure. For II to occur, a high supply voltage is needed and makes the structure to exhibit high electric field which leads to hot carrier degradation effects [6-7]. The effect of hot carrier degradation will damage the gate oxide, which is inconvenient for a transistor performance.

Vertical IMOS was introduced to overcome the hot carrier degradation effect. The structure of vertical IMOS is similar to the gated triangular barrier diode, which is also known as planar doped barrier FET (PDBFET) with a floating body [8]. The hot electrons in the vertical IMOS are spread to the bulk which is contradicted with the hot electron in CMOS that is injected to the gate oxide which in turn damaging it. The hot carrier is reduced when the electrons that passes the δp+ barrier become hot carriers by being accelerated in the high electric field are driven away towards the drain side of the channel region instead moving to the gate oxide [9]. Thus, the hot carrier cannot cause a shifting of threshold voltage because the hot carriers is not injecting to the oxide [9].

Unlike planar IMOS that works on the avalanche breakdown mechanism [9], the vertical IMOS has floating body that will be charged by the holes generated during impact ionization in which will cause a dynamic reduction of the threshold voltage leading to the steep rising of subthreshold slope. Significantly, the device is able to reduce the supply voltage which is the hot electron is damaged almost completely [9-10] and shows the capability of the devices working properly under high temperatures [8]. Therefore, it is observed that the vertical concept of IMOS is better than the planar IMOS in reducing the hot carrier degradation effects.

Computer simulation is a computer process where the computer solves large equation sets, which is describing the connections between circuit elements and the models [11]. As MOSFET devices are scaled to meet increasingly demanding circuit specifications, process variations has a greater effect on the reliability of circuit performance [12]. For this reason, statistical techniques are required to design integrated circuits with maximum yield. The estimation of
the functional yield of a designed circuit without fabrication of the device could be done. Besides that, it is useful in determining the sensitivity to scaling of existing circuits as well as to predict performance variations in new designs.

A circuit model can be comprised of many devices such as resistor, capacitor, MOSFET and/or bipolar junction transistor. A device model is employed to describe the behavioral characteristics of the device with respect to its terminal and comprised with large number of equations. Thus, the equivalent circuit model of vertical IMOS is proposed so it can be used in circuit simulations. This can lead to the new environment of transistor applications in circuit.

II. DEVICE MODEL CONCEPT AND THE EQUIVALENT CIRCUIT MODELING

A. The device model concept for Vertical IMOS

Vertical IMOS is based on a so-called gated triangular barrier diode because of its triangular-shaped potential barrier that is known as a planar-doped barrier MOSFET (PDBFET) [13].

Vertically, drain current rises because of the impact ionization and also the floating body effects. Avalanche breakdown occurs because of the intrinsic silicon layer which acts like a channel when a certain voltage is applied. Intrinsic silicon is an intrinsic semiconductor where the number of electrons and holes has the same amount. When the gate voltage and drain voltage is applied, the electrons from the source region will have enough energy to jump out from their valence band. So, the electrons will move faster through the intrinsic silicon, which acts as a channel and make the flow of electrons is easy towards the drain region. Besides that, high doped δp+ layer also helps to increase the electron mobility towards the drain region for electron-hole pair process. As the drain voltage increase, more electrons will surpass its band gap energy and move towards the drain region and create currents. Hence, the impact ionization will occur. The electron mobility in the drain region is higher than the electron mobility in the source region [14].

The circuit concept is taken from the Electrostatic Discharge (ESD) protection device circuit [15]. This protection device circuit is made to prevent the higher current due to the increase in supply of drain voltage [16]. This is because of the supply high drain voltage makes the device to experience high current and a high electric field is induced. The high current is due to the impact ionization that can make the device unstable. Increasing of drain voltage in avalanche breakdown makes the device enter the snapback breakdown [17-18]. This is due to the second order effects where the breakdown process is called as ‘Near Avalanche and Snapback Breakdown’ [19]. This second order effect is caused by the continuation of avalanche breakdown because of the increasing of supply voltage and called as snapback breakdown.

Most think that the avalanche breakdown occurs because of a particular voltage. However, avalanche breakdown is actually a gradual process that occurs or starts at low current levels and also the electric fields below the breakdown field. As the avalanche breakdown rate increases, the number of carriers in the drain space charge region increases and generates the positive feedback mechanism [19-20]. When this mechanism starts, the substrate acts like a n-p-n (Bipolar Junction Transistor) BJT. Actually, vertical IMOS have a structure like n-p-n BJT because of the same floating body structure. The device is then working under forward-active mode, where the forward biased substrate-to-source junction (base-to-emitter junction) causes a large current to be injected into the p-type substrate (base) [21]. The current is amplified in the substrate region (base) and collected from the drain (collector) through the reverse biased drain-to-substrate junction (collector-to-base junction) [22].

As mentioned earlier, Vertical IMOS has a structure like n (source) – p (substrate) – n (drain) which also forms a parasitic bipolar transistor as shown in figure 1. When the snapback breakdown occurs, large current is created in the substrate and the voltage applied to the gate electrode loses control over the current flow in the channel region, which causes the device to stop functioning. Thus, the equivalent circuit model for vertical IMOS is build based on the concept from the ESD protection device circuit.
The concept of this vertical IMOS still used MOSFET configurations because of the drain, gate, substrate (p+ delta layer), and source structures as shown in figure 2(a). The equivalent device model of the vertical IMOS is shown in figure 2(b). The drain terminal is connected to the collector, while the source terminal connected to emitter. The substrate or the body of the MOSFET is connected to the base of the BJT. This is because the structure of BJT that have a floating base. By connecting the body of the MOSFET to the base of the BJT makes the equivalent circuit model has a floating body like in the device. Figure 2(b) also shows the connection of the basic Vertical IMOS which is not include the structure of the dual intrinsic silicon layer. This is because there is no parameter included in MOSFET or BJT part model in the circuit equivalent. The structure will be discussed further in the next section.

**B. The Device Parameter of Vertical IMOS**

Figure 3 shows the schematic drawing of device structure of the Vertical IMOS. This schematic drawing is used as a reference to design the circuit structure in PSPICE. Besides that, this drawing is also use for the fabrication process that has been proposed by U. Abelein (2006). From U. Abelein experiment value [12], the parameters were extracted and it is used for the equivalent circuit model later. The source electrode is growing with n+ doped silicon of antimony (4x10^8 cm^-3). Then, it is designed to stack the intrinsic silicon layer with a concentration of doping <10^6 cm^-3 followed by a highly boron doped 3nm δp+ layer with concentration <10^9 cm^-3 and again 40nm intrinsic layers. So, the channel length of this structure is Lch=83nm because of channel length is measured from the source to the drain. The drain is phosphorus doped n+ silicon layer (4x10^8 cm^-3). The thickness of the gate oxide also considered. A 4.5nm of gate oxide is thermally grown.

**C. Device modeling of Vertical IMOS**

A vertical IMOS model is developed by using ORCAD PSPICE circuit simulation software. The MOSFET model parameter used level 3 because of the sensitivity towards the threshold voltage [23] which is useful to determine the threshold voltage which is needed for the Vertical IMOS to have a low threshold voltage. Besides that, the BJT model used the default value that was given in a set of parameter in the PSPICE software. ORCAD PSPICE software used the Monte Carlo model to perform the circuit simulations. Monte Carlo and sensitivity/worst case analyses are statistical and it is used in PSPICE software for simulations. PSPICE changes device model parameter values with respect to device and lot tolerances that had been specify, and runs a simulation for each value.

The model of the electronic circuit is represented by the electrical properties and characteristic of each component used. The characteristic graph (Ids-Vgs) of the device modeled will be compared with the experimental value of Vertical IMOS proposed by U. Abelein [11].

The level 3 of MOSFET model parameter is set as the equations below. To calculate the threshold voltage, \( V_{TH} \)

\[
V_{TH} = V_{EG} - \frac{\gamma}{\beta_{f}} + V_{FB} + \frac{V_{FB}}{2} - \frac{2\Phi_{F}}{\gamma} - \frac{2\Phi_{F}}{\gamma + \Phi_{S}}
\]

(1)

where \( \gamma = \frac{2(\Phi_{F} - \Phi_{S})}{\Phi_{F}} \)

(2)
The body factor is symbolized as $\gamma$, while $V_F$ is the bulk Fermi potential. $F_s$ is a short channel factor and $F_w$ is a narrow width factor. For the current ON to be obtained from the graph is in the linear region where the equation for drain current;

$$I_D = \beta(V_{GS} - V_{TH} - \frac{L}{2}F_sV_{DS})V_{DS}$$  \hspace{1cm} (3)

where $\beta = \frac{W}{L} \mu_{eff} C_{ox}$ \hspace{1cm} (4)

$$F_s = Taylor \ series \ expansion \ coefficient \ of \ bulk \ charge$$

For current OFF, the graph show at the subthreshold region, where $V_{GS} < V_{COV}$

$$I_D = I_D \exp \left( \frac{1}{4\hbar^2} \frac{V_{GS} - V_{COV}}{E_F} \right)$$  \hspace{1cm} (5)

where $V_{COV} = V_{TH} + \frac{nF_s}{2}$ \hspace{1cm} (6)

$$n = 1 + \frac{NFS}{C_{ox}} - \frac{SN}{C_{ox}}$$ \hspace{1cm} (7)

$I_D$ is the value of $I_{ON}$ where $V_{GS} = V_{COV}$ by using equation (3), NFS is the fast surface state density where its necessary to invoke the weak inversion feature and $C_D$ is depletion capacitance [22-24].

The model incorporates three additional resistors which are $R_g$, $R_s$, and $R_d$ used to account losses at the gate, source and drain respectively. Most of the drain resistance is accounted by the resistance of the main body on the n$^+$ region, although the metal contact in this region meets the thinner inversion region which also contributes to this resistance [25].

As the scaling of the MOSFET enters the micrometer regime, the effects of the drain and source resistance on the overall device performance must be observed carefully. It is known that the $R_s$ and $R_d$ exhibits gate bias dependence in MOSFETs [26]. The device electrical performance and reliability, saturated drain current ($I_{ON}$), trans-conductance ($g_m$), noise figure, cutoff frequency and hot carrier degradation effects depend more on $R_s$ rather than $R_d$ [27]. Lastly, the gate-source and drain-source voltage ($V_{gs}$ and $V_{ds}$ respectively) is applied to the circuit used for the capacitor while $V_{dd}$ is set to 5V. The extrinsic resistances ($R_g$, $R_s$, and $R_d$) are used to enhance the fitting quality to the high frequencies.

Intrinsic layer is not represented in the set of parameter in MOSFET or BJT model in the PSPICE software circuit simulation. So the intrinsic layer must be located according to the device structure of vertical IMOS. The intrinsic layer which is an oxide layer is represented by locating the capacitor, $C_{11}$ between the drain and body, while the second capacitor, $C_{12}$ represents the second layer is located between the body and source.

Other than that, the intrinsic capacitances which are covered by PSPICE, there is also great overlaps and fringing capacitances in vertical MOSFET. Figure 4 shows the parasitic overlap and fringing capacitance in vertical MOSFET. It is also considered for the vertical IMOS which is expressed as gate-source capacitance, $C_{gs}$ and gate-drain capacitance, $C_{gd}$ because of the similarity of the structure with vertical MOSFET.

### III. RESULTS AND DISCUSSIONS

The circuit consists of the equivalent circuit model of vertical IMOS (contains of n-MOSFET and NPN BJT), some parasitic elements which are capacitances and resistors as a basic component as shown in figure 5. This equivalent circuit shows the performance of Vertical IMOS in circuit representations. The parameter of the device modeled is fixed as it has been used from the experimental value. The substrate doping or the concentration of the floating body of vertical IMOS (NSUB) of $\sim$10$^6$ cm$^{-2}$, oxide thickness (TOX) of 4.5nm, channel length (L) of 83nm, threshold voltage obtained from the referred experimental value (VTO) of 1.3V, and ideal width (W) is fixed to 1000nm approximately.
Vertical IMOS are working in different operations, unlike the planar IMOS. There are three modes of operation occur in vertical IMOS [12]. First, conventional MOSFET (CMOS), second, Impact Ionization (II) and lastly, Bipolar Junction Transistor (BJT) mode. These modes are determined by the drain voltage applied to the device.

Figure 6 shows the graph of transfer characteristic that was obtained from the equivalent circuit and device modeling analysis. For $V_{DS} \leq 1.5V$, the device acts like CMOS. At this rate, there is not enough energy for the II to occur. The subthreshold slope observed is 76.58mV/dec at $V_{DS}=1.25V$, while at $V_{DS} = 1.5V$, the subthreshold slope is 72.89mV/dec. When $V_{DS}$ is 1.75V, the device is starting to have enough energy for II to occur. At this mode, the subthreshold slope of the device is observed is 18mV/dec which is lower than the limit value of subthreshold slope for CMOS. Continuing of supply gate voltage makes the devices turn into BJT mode.

Figure 7 shows the comparisons of the experimental value obtained by U. Abelain (2006) with the PSPICE simulation obtained from this research. It is observed that the current ON and the current OFF almost have same result which is when the device turned ON at $V_{DS}=1.75V$, the $I_{ON}$ is $10^2$µA/µm and $I_{OFF}$ is $10^{-7}$ µA/µm. The circuit equivalent model shows the $I_{ON}/I_{OFF}$ ratio of $10^9$µA/µm which is higher than the referred experimental value. The subthreshold slope also is seen to have much slightly lower than the experiment one. The similarity percentage of the PSPICE simulation with the experimental value is 90%. The data are also tabulated for clear comparisons as shown in the Table 1.
The circuit equivalent model for Vertical IMOS was proposed and has been analyzed with the previous work for the validation. Also, the circuit obtained is based on the ‘Near Avalanche and Snapback Breakdown’ mechanism. Other than that, the device modeling of the Vertical IMOS was analyzed and the results were obtained by using the ORCAD PSpice software. The parameter extraction of the device may be used for the new invention of equation sets. The device modeling shows almost have similarity between the experimental values by U. Abelein (2006) with the data environment to complete this work.

### IV. Conclusions

The circuit equivalent model for Vertical IMOS was proposed and has been analyzed with the previous work for the validation. Also, the circuit obtained is based on the ‘Near Avalanche and Snapback Breakdown’ mechanism. Other than that, the device modeling of the Vertical IMOS was analyzed and the results were obtained by using the ORCAD PSpice software. The parameter extraction of the device may be used for the new invention of equation sets. The device modeling shows almost have similarity between the experimental values by U. Abelein (2006) with the data obtained from this research. The performance analysis of the subthreshold slope value of PSpice simulation with the reference value shows that 90% of similarity. It is also shown that the $I_{ON}/I_{OFF}$ ratio from the PSpice simulation with the reference experimental value have almost the same value which is the PSpice simulation is slightly have higher value. Thus, the circuit simulations of vertical IMOS can be used and further study is needed for vertical IMOS transistor in terms of biosensor applications.

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### REFERENCES


