Mitigation of Voltage Flicker using Phase-Lock Loop (PLL) Controller of Distribution Synchronous Static Compensator (D-STATCOM)

Nur Fadhilah Jamaludin  
Faculty of Electrical Engineering  
Universiti Teknologi Mara,  
Permatang Pauh, Pulau Pinang, Malaysia  
nurfadhilah2765@ppinang.uitm.edu.my

Ahmad Farid Abidin  
Faculty of Electrical Engineering  
Universiti Teknologi Mara, Shah Alam, Selangor, Malaysia  
amhad924@salam.uitm.edu.my

Norhasnelly Anuar  
Faculty of Electrical Engineering  
Universiti Teknologi Mara, Permatang Pauh, Pulau Pinang, Malaysia  
norhasnelly@ppinang.uitm.edu.my

Sarah Addyani Shamsuddin  
Faculty of Electrical Engineering  
Universiti Teknologi Mara, Permatang Pauh, Pulau Pinang, Malaysia  
sarah.addyani@ppinang.uitm.edu.my

Abstract — The negative impact of power quality problem due to voltage flicker has gained a growing concern from utilities, especially in the areas of distribution planning. The EAF is observed to produce the most common severe voltage flicker in the industrial systems due to it random and stochastic characteristics. Thus, this paper has proposed a new controller for 6-pulse D-STATCOM based on Phase-Locked Loop (PLL) controller with Hysteresis Current Control (HCC) switching to mitigate voltage flicker in power system. The IEEE 6 bus distribution system has been used to analyze the capability of the proposed techniques. The simulation result shows that the linearity that exists in this proposed controller has a capability to mitigate voltage flicker at different frequencies below the maximum permissible curve level.

Keywords - Electric Arc Furnace, Flicker, Phase-Locked Loop, Hysteresis Current Control

I. INTRODUCTION

Flicker is considered as one of the most severe power quality problems due to the proliferation of non-linear varying loads [1]. It is a difficult problem to quantify and solve due to the subjective nature that involved human factors. It is noticed that, the voltage flicker with frequency variation from 1 Hz to 10 Hz can cause the incandescent lamps and the television picture to glitter thus may induce discomfort in the form of nausea, headaches, annoyance, distraction, feeling of tiredness and problems with concentration for the people exposed to it and hence affect the production environment [2]. In addition, voltage flicker also may subject the electrical and electronic equipment to detrimental such as reduction of efficiency of electrical equipment, power oscillations, and interferences in protection systems [3].

The EAF is observed to produce the most common severe voltage flicker in the industrial systems due to it random and stochastic characteristics [4]. It is noticed that for flicker frequencies varies from 0.1 Hz to 30 Hz, the EAF consumes considerable time-varying, stochastic, and chaotic characteristics of reactive and real power during it process. These large and erratic swing of reactive current produce voltages drop in the system impedance of the AC system resulting in fluctuating voltage at points of common coupling [5].

Therefore, it is important to reduce the negative effect of voltage flicker. Various mitigation techniques has been proposed by previous researchers to reduce the flicker level below maximum permissible limit such as (a) decreasing the furnace power, (b) increasing the short-circuit power at the point of common coupling and (c) installing compensators [6].

The first option is not acceptable for customer since it will reduce the arc furnace capacity meanwhile; the second option can only be applied at design stage. The last option is the most commonly used by previous researchers to compensate voltage flicker in power system into perceptible level [7].

The D-STATCOM based on the Voltage Source Inverter (VSI) is considered as a suitable flicker mitigation technique that performs better than Static Var Compensator (SVC) with fast time response and flexible control. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of reactive and real power exchanges between the D-STATCOM and the AC system [8]. However, the performances of D-STATCOM depend on the effectiveness of the control algorithm that has been used to extract the references voltage or current components to compensate the voltage flicker in power system.

Various IRP algorithms using p-q method with Sinusoidal Pulse Width Modulation (SPWM) for D-STATCOM have been reported in [9-11]. The Instantaneous Reactive Current loop has capability to generate references reactive current that will be used as an input in current control loop for switching purposed. The combination of both control loops allow the flicker components are correctly detected and hence reduce the flicker level at the entire interconnected load. Nevertheless, this method has too many calculation demands for the p-q conversion. In
addition, the existing of High Pass Filter (HPF) in inner loop will introduces magnitude and phase errors. Moreover, the repetitive adjustment of Proportional Integration (PI) parameters values in takes a considerable effort in order to obtain perfect sinusoidal voltage waveform [11].

The new IRP algorithm techniques has been proposed in [12] and [13]. This technique accurately extracts the three phase instantaneous positive-sequence current of base frequency. Through this technique, any time instant can be chosen as the starting point for current compensation, regardless of the phase information of the three-phase voltages or current. It is thus gives a feasible solution to the IRP compensation regarding intensive nonlinear or quasistochastic loads especially arc furnace. However, the deficiency in term of time response still can be observed due to the used of Low Pass Filter (LPF) during instantaneous reactive and real power filtering process.

The voltage flicker mitigation based on SRF algorithm using direct- quadrature (d-q) method with SPWM switching have been widely used by previous researchers in [14-16]. This technique involved the decoupling between the reactive and real power loop where may degraded when the unbalanced factor increase especially during melting process of arc furnace thus worsen the performances of D-STATCOM.

Another modified SRF algorithm has been introduced [17]. This method is similar to the previously SRF method but differ in term of voltage and current generation. In this technique, the generating of voltage and current are taken from the nonlinear load instead of PCC. This technique has capability to stabilize voltage at PCC and compensated the negative sequence component of the voltage vector. Nevertheless, the existing of two HPF components in this method to filter fluctuation reactive and real signal will affect the time response of the control system.

From the cited references, it is found that the mitigation of voltage flicker in EAF have gained numerous concerns from previous researcher. Various control techniques for D-STATCOM reported in the literature are facing the problematic in term of delay in time response, non-linearity algorithm, unbalanced of DC voltage and complex configuration. This paper present new technique to mitigate voltage flicker based on PLL controller with HCC switching for 6-pulse D-STATCOM. It will be demonstrated that the capability of this techniques to inject the reactive power at point of common coupling (PCC) thus reduce the flicker below maximum permissible limit. The IEEE 6 bus test system is used to ascertain validity of the proposed techniques which will be discussed in details in the next following sections.

II. ELECTRIC ARC FURNACE MODEL

In order to take the precautions on minimizing the adverse effects of arc furnaces, it is necessary to develop an accurate EAF model. However, the development of an electric arc model is a very challenging task due to the complexity of the arc furnace physical phenomena and the randomness associated with arc furnace operation [18].

Therefore, in this study the deterministic EAF model in [19] is used to create voltage flicker in power system. This arc furnace model is developed from the energy balance equation which is actually a nonlinear differential equation of arc radius and arc current as in equation (1).

\[ k_d r^2 (t) + k_d r(t) (dr/dt) = \left( \frac{k_3}{r^{m+2}(t)} \right) i^2 (t) \]  (1)

The arc voltage is given by equation (2)

\[ v = Ri = \left( \frac{k_3}{r^{m+2}} \right) i \]  (2)

Where:
- \( r \) is the arc radius
- \( R \) is the arc resistances
- \( i \) is the arc current
- \( v \) is the arc voltage
- \( k_3 \) is the arbitrary constant (\( n = 1, 2, \text{ or } 3 \)).
- \( m \) is arc constant to reflect that the arc may be hotter in the interior if it has a larger radius (\( m = 0, 1, 2, \text{ or } 3 \)).
- \( n \) is the arc cooling constant (\( n = 1, 2, \text{ or } 3 \)).

The simplified V-I arc characteristic can be find by using equation (1) and (2) as presented in Figure 1. It has been noticed that, once the arc ignition has been started, the anode-cathode voltage remains constant while the current is still changing in time.

![Figure 1. V-I Arc Characteristic using the Mathematical Model](image)

Through this model, the V-I operating characteristic of arc furnace are obtained accurately by properly modifying the parameters of \( m \) and \( n \). In this study, the corresponding \( m \) and \( n \) parameters are chosen as \( m=0 \) and \( n=2 \) to represent the melting stage as indicate in [19] and [20]. The arbitrary constant value of \( k_1 \), \( k_2 \), and \( k_3 \) in existing EAF of PSCAD/EMTDC model has been determined by trial and error to tune the worst voltage flicker at different flicker frequencies range. Therefore, for the purpose of this study, the value of \( k_1= 2750, k_2 = 1 \text{and } k_3 = 15.5 \) are selected to create the worst voltage flicker at PCC.
The usual method for expressing flicker is similar to the percent voltage modulation. It is noticed that, the flicker is usually expressed as a percent of the total change in voltage with respect to the average voltage, $\frac{\Delta U}{U}$ over a certain period of time as expressed in equation (3).

$$\Delta U/U = \left(\frac{U_{\text{max}} - U_{\text{min}}}{(U_{\text{max}} - U_{\text{min}})/2}\right) \times 100\% \quad (3)$$

$$= \left(\frac{U_{\text{max}} - U_{\text{min}}}{U_{\text{nom}}}\right) \times 100\%$$

Where:
- $U_{\text{max}}$ is the maximum voltage value
- $U_{\text{min}}$ is the minimum voltage value
- $U_{\text{nom}}$ is the average value of normal operating voltage

The amount of voltage flicker as calculated in equation (3) will verify either flicker cause the irritation to the system or not. If the percentages of voltage flicker within the borderline of irritation curve thus it is indicates the flicker begins to objectionable by people. When this occurs, the appropriate flicker mitigation technique is needed in order to reduce the voltage flicker below permissible thresholds limit.

### III. MODELING AND CONTROL TECHNIQUES

A D-STATCOM is basically consists of a step-down transformer with a leakage reactance, a three-phase IGBT VSI with DC capacitor and control system as shown in Figure 2. The voltage difference across the leakage reactance produces reactive power exchange between the D-STATCOM and the power system, such that the AC voltage at the bus bar can be regulated to improve the voltage profile in the power system [21].

![Figure 2. Single Line Diagram of D-STATCOM](image)

As indicate in Figure 2, when VSI output voltage, $U_{\text{vsi}}$ is greater than the AC voltage source at PCC, $U_{\text{pec}}$ the D-STATCOM notify that the system is in inductive condition. The current, $I$ flows through interface reactance, $X$ from the AC system to the D-STATCOM. Meanwhile, if the AC voltage source at PCC, $U_{\text{pec}}$ is greater than the VSI output voltage, $U_{\text{vsi}}$ the D-STATCOM give an indication that the system is in capacitive condition. The current, $I$ flows through the transformer reactance, $X$ from the AC system to the D-STATCOM. Hence, if the amplitudes of system and inverter voltage are equal thus no power exchange takes place [12]. This flowing current, $I$ is basically can be expressed in equation (4).

$$I = \left(\frac{U_{\text{pec}} - U_{\text{vsi}}}{X}\right) \quad (4)$$

From equation (4.1), it is shown that the reactive current, $I$ drawn by synchronous compensator is determined by the magnitude of the AC system voltage, $U_{\text{pec}}$ the inverter voltage, $U_{\text{vsi}}$ and transformer leakage reactance, $X$ in order to determine the capability of D-STATCOM to inject or absorb reactive power to or from the power network. As a result, this prevents the oscillating voltage and current flow through the power network and reduce the voltage flicker into below maximum permissible voltage fluctuation curve [12].

#### A. Voltage Control System

The proposed control techniques for 6-pulse D-STATCOM are based on the extraction of unit vector templates without using any transformation for generating the references voltage to mitigate the reactive power which is absorbed or released by EAF load [22, 23]. The employed control strategies consist of two control loops as shown in Figure 3.

![Figure 3. The D-STATCOM Controller based on Unit Vector Templates Generations](image)

The first control loop based on the extraction of the three phase voltage fluctuation at PCC. The PLL will utilize the voltage at PCC as references in order to generate the phase angle for the references source current. Equation (5), (6), and (7), show the combination of PLL output and phase...
shift which being used to generate three phase unity sinusoidal references source currents.

\[
\begin{align*}
U_{PCC}*A &= \sin (\theta) & (5) \\
U_{PCC}*B &= \sin (\theta - 120^\circ) & (6) \\
U_{PCC}*C &= \sin (\theta + 120^\circ) & (7)
\end{align*}
\]

The second control loop which known as DC voltage control loop. This voltage control loop is employed in order to determine the peak value of the references source current, \(I_m\). The PI controller will determine the part of the fundamental references source current, \(I_{mref}\) by comparing the measured DC voltage, \(U_{dc}\) with a references DC voltage, \(U_{dcref}\). The output of this PI controller is then being added with a constant that equal to the peak magnitude of the fundamental PCC current, \(I_{fpcc}\) in order to determine the magnitude references source current, \(I_m\). The peak value of the references source current, \(I_m\) is then being multiplied with the equation (5), (6) and (7) to obtain the references source current signals, \(I_{ref}\) for each phase as derived in equation (8), (9) and (10).

\[
\begin{align*}
I_{refA} &= U_{PCC}*A \sin (\theta) * I_m & (8) \\
I_{refB} &= U_{PCC}*B \sin (\theta - 120^\circ) * I_m & (9) \\
I_{refC} &= U_{PCC}*C \sin (\theta + 120^\circ) * I_m & (10)
\end{align*}
\]

These references source current signals are used as the input for the inverter switching process which will be discussed in detail in the following section.

B. PWM Using Hysteresis Current Control (HCC)

HCC for the control of D-STATCOM is used in this study is insensitive to system parameters with inherent peak current limiting capability, simple to be implemented and has capability to reduce the low order harmonic content of the VSI output current. The effectiveness of the D-STATCOM depends on its ability to follow the references signals with minimum error to compensate the voltage flicker within allowable band.

Figure 4 shows the general schematic diagram of the proposed HCC operation used in this study.

The hysteresis comparator output with suitable band (±h) will decide the switching pattern of the inverter. The source current, \(I_s\) is compared with a references source current, \(I_{ref}\) in order to obtain the error current signal, \(I_{error}\). This error current, \(I_{error}\) will pass through three fixed hysteresis comparators to activate the inverter power switches. It is noticed that, the gate, \(G_n\) will send 0 logic value to turn OFF the upper switch in the half-bridge and turned ON the lower switch if the source current signal, \(I_s\) exceeds a predefined hysteresis band (HB). Meanwhile, if the source current, \(I_s\) reaches the goes below the HB, the gate, \(G_n\) will send 1 logic value to turn ON the upper switch in the half-bridge and turned OFF the lower switch [12, 24].

IV. SIMULATION RESULTS

In this paper, the IEEE 6 bus test system as illustrated in Figure 5 is used to validate the performance of the proposed technique.

The IEEE 6 bus system is non-radial power system that consists of 220 kV power network which is supplied by two 11 kV generators [25]. The simulation models of the system are developed by using PSCAD/EMTDC software tools. Generators are modelled by using three-phase voltage source while the transmission lines are modelled based on resistance- inductance (RL) component. The fixed load model for both resistive and inductive load is used for system loading with 50 Hz of operating frequency system.

The connection of the 25 MVA of EAF loads that located between the two generators as shown in Figure 5 will produced the severe erratic current swings and hence created stochastic EAF voltage as shown in Figure 6. This EAF also will lead to the variation of reactive and active power drawn by EAF load as illustrated in Figure 7.
HCC control has been connected at bus 2. The connected of this compensator with the proposed controller have capability to ensure the converter absorbs a small amount of real power at nearly null value and deliver sufficient reactive power to the AC system to mitigate voltage flicker as shown in Figure 9. Figure 10 show that the injection of reactive power at bus 2 will stabilize the voltage by reducing the percentage of fluctuation from 2.7925 % to 0.2559 %. This is thus resulting the percentage of voltage fluctuation is below the maximum permissible level of 2.10 %.

Figure 6. Voltage at EAF Load at 10 Hz Flicker Frequency of IEEE 6 Bus Systems

Figure 7. The Reactive and Real Power Consumed at Bus 2 to run The Operation of EAF

This large variation of reactive power that flow between buses 2 will cause the voltage flicker in power system as shown in Figure 8. Therefore, by using equation 3, it has been noticed that the percentage of voltage fluctuation at bus 2 is 2.7925 % which is exceeded the permissible limit of 2.10 %.

Figure 8. Voltage Flicker at Bus 2 without Mitigation Device at 8.8 Hz Flicker Frequency

Therefore, in order to mitigate the voltage flicker in power system, the 6-pulse D-STATCOM with the PLL and
improve the power system productivity.

voltage flicker at PCC, but also manage to mitigate voltage reactive power to the system and hence stabilized power developed based on the robustness of PLL controller with mitigation due to EAF. The proposed technique is based on the Robustness of PLL controller with supports from Universiti Teknologi MARA (UiTM) for its technical aspects. The technique involves the use of a DSTATCOM, as reported in [1].

The technique was validated using data from [2], [3], and [4]. The results show a significant improvement in voltage flicker mitigation. The technique was further validated using data from [5] and [6]. The results showed a consistent improvement in voltage flicker mitigation.

V. CONCLUSION

This paper proposed a new technique for voltage flicker mitigation due to EAF. The proposed technique is developed based on the robustness of PLL controller with PWM. The technique was validated using data from [7] and [8]. The results showed a significant improvement in voltage flicker mitigation.

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REFERENCES


