A 27GHz Frequency Divider in 0.18µm CMOS Technology

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Abstract — This paper presents a broadband high operating frequency divide-by-2 frequency divider. This divider uses source-coupled logic (SCL) with two static loading master-slave D latches which achieves high input operating frequency, high input sensitivity and low power dissipation. This divider can work from 8GHz~27GHz and the input power is -40dBm@18GHz. The chip area is 735µm×480µm with only 4.6mW power dissipation at 27GHz input working frequency and 1.8V power supply.

Keywords – broadband - frequency divider; source-coupled logic (SCL); static-loading; input-sensitivity; CMOS

I. INTRODUCTION

Frequency divider (FD) is one of the kernel parts of phase-locked loop (PLL) in conventional high speed transceivers. To design low power, wide band and high speed modules in radio frequency systems, integrated circuits tend to work at higher frequency, lower power dissipation. Despite frequency and power dissipation requirements, the FDs turn to work at lower input sensitivity. Due to the continuously decreasing feature size and increasing fT, FD chip size is decreasing and the level of integration is getting higher and the supply voltage is lowered, too. However, new challenges are existed.

There are many topologies for CMOS FDs, such as source-coupled logic (SCL)/current-mode logic (CML), regenerated and injected-locked frequency dividers (ILFDs) [1-3]. Static SCL FDs are considered the main structure below 10GHz working frequency. Static CML/SCL FDs have been normally used from 10 GHz to 40 GHz working frequency. From 40GHz to 100GHz working frequency, ILFD structure is widely used because of the limit of today’s standard CMOS process [2]. This paper presents a static SCL divide-by-2 FD which achieves 8-27GHz working frequency using TSMC 0.18µm CMOS technology. The proposed divider achieves both a wider input locking range and lower power dissipation at 1.8V supply voltage. What’s more, the input amplitude is lower comparing to similar FDs in 0.18µm CMOS process [4-5].

II. FREQUENCY DIVIDER TOPOLOGY

A conventional static SCL FD divide-by-2 proposed by Wong is shown in Fig. 1 where two cascaded static SCL latches with unity-gain bandwidth optimized are used in the master-slave structure [6]. If the Vgs of input differential pair is increased, the unity gain bandwidth fT will increase, which means that W of the differential pair will decrease for a given ID [6]. If vary width and length of a poly resistor which is directly proportional to the load resistance, it is verified that fT is relatively constant over different length and fT increases as width decreases. However, values of width and length which are too small influence less than unity voltage gains and thus fT drops quickly. As a result, it is reasonable to slightly oversize width and length of the resistor pair to tolerate process variations.

Due to the parasitic capacitance of the sample part, the tail current must be set very high to achieve wide range of linearity, large transconductance and high slew rate. The hold part shares very small bias current. However, these characteristics cannot be reconciled in normal SCL latch design because there is only one single constant current source in it. It is possible to simplify the normal SCL latch circuit by using a single clock transistor pair as a switch to control the current between the sample and hold part of both the master and slave latches [7]. Because of the limitation of CML structure and the fT of fabrication process, the highest operating frequency of the static CML structure FD is almost fixed to half of the fT. In order to increase the operating frequency, ILFD FD and SCL FD with passive devices are accepted.

Each latch is composed of a pair of static resistor loads (R1, R2), a pair of sample transistors (MS1, MS2) and a pair of regenerative hold transistors (MH1, MH2). Voltage controlled oscillator (VCO) provides FD’s differential output signals input signals IN+ and IN−. When IN+ is low, MC1 and MC2 in master latch I are “1” and latch I is in sample mode, while MC1 and MC2 in slave...
latch II are “0” and latch II is in the hold mode. When IN+ goes high, MC1 and MC2 in latch I are “0” and the master latch is in hold mode. Comparing to dynamic SCL structure, static SCL FDs use pure static resistance loads instead of active transistor loads. It is verified to have good noise performance and it is easier to choose the size of pure static resistance load than appropriate dynamic resistance load that used in dynamic SCL topologies for the reason as follow.

The noise of this FD comes from white noise and licker phase noise, because only the second latch noise sources need to be considered in output jitter assessment[8]. The second latch jitter at the output is not affected by the first latch noise because the output signals is not controlled by the latch. As a result, the jitter can be computed from the variance of output voltage as in Ref:

\[ \sigma_{j}^{2} = \frac{V_{j}^{2}}{S_{j}} \]

where \( S_{j} \) is the slope of the output voltage at the zero crossings. The period jitter (\( \sigma_{j}^{2} \)) is computed as

\[ \sigma_{j}^{2} = S_{j}^{2} + \sigma_{j}^{2} \]

According to the expression \( \phi = 2\pi f_{out} t_{0} \), the phase of the output signal is sampled at \( f_{out} = 1/T_{out} \) and it is proportional to the switching instant. The sampling process folds back any noise component at frequency higher than \( f_{out}/2 \) and the phase spectrum is defined in the Nyquist band 0.

Then, the time jitter can be written in terms of the integral of the single-sided power spectral density (PSD) of the phase within the Nyquist band:

\[ \sigma_{j}^{2} = \frac{1}{4\pi^{2} f_{out}} \int_{0}^{f_{out}/2} S_{\phi}(f) df. \]

B. The Proposed Static SCL FD

In this work, the effort is focus on how to increase input sensitivity of static SCL. In some applications the input power of FD can not be so high for low power application, comparing to dynamic SCL FD, the static SCL topologies can achieve higher input sensitivity and can work at reasonable power dissipation. Two differential spiral inductors which are connected in series with the 50Ω testing source are adopted in this FD. They can resonate with the input parasitic capacitances (R1/R2, MC1/MC2) and enlarge the effective clock signal amplitude by Q times [9]. Here, Q is about 1.5-2 to relax the inductor design.

Fig. 2 shows the circuit implementation of this high sensitivity static SCL divide-by-2 FD. Similar to conventional static FD, the proposed FD is made of two
latches and each latch has two control devices MC1 and MC2. MC1 and MC2 help to control the latch and shut down the tail current in the latch during half of the clock cycles. It enables the sample transistors (MS1, MS2) and regenerative hold devices (MH1, MH2) are "0" during the hold period, thereby the current become smaller and the output impedances at Q and QB increase during the hold mode.

By using resistor load, it is easy to decide the size of MH1 and MH2 which is very sensitive to the output frequency. When input signal IN+ is "0", the sample part (MS1, MS2) and the hold part (MH1, MH2) in master latch I is "1" and latch I is in sample mode, while the slave latch II is "0" and latch II is in hold mode. When IN+ goes to "1", the reverse applies.

It is important to consider how to optimize FD parameters. Firstly, considering the electronic mobility of MOS transistors of TSMC180nm process and decide the ratio of MS1/MS2 and MC1. Secondly, estimating RC parasitic parameters according to target working frequency then set width and length of MS1/MS2 and MC1. What is more, sweep the parameters and get a better according to oscillating frequency. A cascaded output buffer in Fig. 2(c) has been used to simulate the output signal connecting to 50 Ω external terminals. The first stage buffer is normal differential amplifier while the second stage is source follower with large current flow. The two stage cascaded buffer topology brings larger output drive ability and lower working frequency range limitation.

III. SIMULATION RESULTS

The presented static SCL FD has been realized in TSMC 180nm CMOS process. Fig. 3 is the layout design and the chip size is 735µm×480µm. The input frequency has been swept to get the upper and lower frequency limits. The minimum input clock signal amplitude required for correct operation of divide-by-2 function has been swept to get the input sensitivity. What is more, the power dissipation of the proposed FD is calculated by probing the core current. It is found that the presented static SCL is able to operate at a wide frequency range from 8GHz to 27GHz. Fig. 4 shows the input and output differential signals of the proposed FD at an input frequency of 8GHz and 27GHz. The input sensitivity curve is shown in Fig. 5 and the presented scheme exhibits high sensitivity especially at higher working frequencies. The minimum input power is-40dBm@18GHz. The maximum power dissipation is 4.6mW@27GHz and the minimum power dissipation is 2.35mW@7GHz at 1.8 V supply voltage.
In this paper, a static SCL divide-by-2 FD with low power dissipation and wide working frequency range is presented. Analysis shows that the working frequency range is 8–27 GHz and the input sensitivity is as low as -40dBm@18GHz. The maximum power consumption is 4.6mW@27GHz and the minimum power consumption is 2.35mW@8GHz from a supply voltage of 1.8 V. The simulation results show that the presented static SCL FD is suitable used in PLL block of radio frequency receivers or other ultra-wideband, low power applications.

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REFERENCES