An Efficient SIC Generator using X Filling Techniques for Low Power Scan based BIST

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Abstract - In test-per-scan BIST systems requires a larger test time due to the longer pattern lengths. We proposed an efficient SIC generator with pre selected seed values generated using X filling techniques such that don’t cares are filled using one-fill and zero-fill methods. Finally seeded value is XORed with SIC generated value gives low power test patterns. The novelty of proposed methods is to use minimum test patterns to test high density VLSI circuits and achieved very high fault coverage. This method compared with Bit swapping and LSA-TPG techniques, the results are very effective, this approach decreases the transition activity, dynamic power dissipation and increases the fault coverage.

Keywords - Low power BIST, SIC LFSR, X-Filling Technique, Transition activity, ISCAS Benchmark Testing.

I. INTRODUCTION

In present era of SOC design usually have low controllability and observability and the major challenging problem are performance, testing time, area overhead, reliability and power dissipation during test. Power consumption in test mode is usually 200 % higher than that in normal mode [2]. Whenever the circuits consumes more power many difficulties arises such as increase in the cost of fabrication and testing, reliability of the circuit diminishes, performance will be degraded and the systems become dependent. So there is necessity to reduce the power consumption by circuits to make them more efficient and effective. The source of power dissipation due to increase in transition activity in the applied patterns. To reduce activity among the patterns, seed generator plays in major role. In our proposed method we replace traditional seed generators and uses X-filling techniques. This techniques use to minimize the Hamming distance between primary inputs and primary outputs and useful in power aware and at speed scan testing [1]. To improve controllability and observability we have opted Scan based Built in Self Test (BIST), it is a Design for Testability (DFT) scheme that allows the system to test itself.

Earlier many schemes applied and proposed for scaling down the power consumption. In [1] presents AB-filling algorithms are used to reduce capture power while feeding the first test patterns to DUT. Lee Proposed the built in test patterns are generated by LSA-TPG, which is ExOr with seed generator and obtained 188 mw test power [2]. In [3] proposed algorithm for low power LFSR in which 87.6 mw dynamic power dissipated during test. In above two approaches targeted bench mark is c432 circuit. In [4] LP-LFSR, seed generator is used to test synchronous 4x4 and 8x8 multiplier.

Scan chain method in which the utilization of extra scan chain to reduce the switching activity and it is referred as selective triggering scan architecture proposed in [4]. Scan cell ordering testing technique is proposed in [5]. A dual speed technique for low power BIST describe in [6] [7]. To produce the random single input change (SIC) vectors, a mixture of LFSR and scan shift register is used in [8]. SIC generator technique is an excellent low power approach which greatly reduces the transitions of inputs to decrease the internal transition activities where transition activity directly proportional to testing time, In [10] the combination of LFSR and scan shift registers is used to generate random single input change patterns in this approach take longer time to test. In [11], a pseudo single input change sequence technique is proposed by adding an extra cyclic shift register and XOR gates, so that 2^n-1, n is the size of LFSR, a single input change test vectors can be inserted between two neighbor vectors generated by LFSR. Thus average power is reduced and reduces time of testing. The drawbacks above methods are switching activities will still be very large and using larger test vector to achieve maximum fault coverage and also if the test clock frequency is very high. This paper proposed a novel technique to reduce transition activity with negligible clock frequency here conventional seed generator replace with X-filling technique called Efficient SIC Generator. The rest of the paper is configured as follows. In section II, explains background which describes scan design architectures and ISCAS benchmark circuit specifications. The Hardware implementation details are discussed in section III. In Section IV describes result analysis and finally outlines the conclusion in Section V.
II. BACKGROUND

A. Scan Design Architecture

The basic principle of testing is Automatic test pattern generator used to apply test vectors to Device under test (DUT) and output from DUT compared with golden signature, if the output of DUT match with signature, device is pass otherwise fail as shown in figure 1. To validate effectiveness of the proposed designs the International Symposium for Circuits and Systems (ISCAS) has designed certain DUT called as the benchmark circuits that are extensively used in DFT.

In scan design-based DFT, the flip-flops a sequential logic circuit are converted into a shift register by adding a multiplexer to the input of each flip-flop. Flip flop (FF) to scan flip flop (SFF), it can be observed in generated netlist. and benefits are highly automated process, highly-effective, predictable, method, assured quality and ease of use, The main purpose to improve controllability and observability of VLSI circuits and also this technique used for minimizing shift and capture power during scan testing without any lose of fault and test coverage, The figure 2 describes combinational circuit with scan flip flop where Scan enable SE used to change circuit in normal mode (SE=0) and scan mode (SE=1), it can operate using 2 to 1 MUX, SE =0, Q=D and SE=1, SI=SO and figure 3 shows full scan design as explain above.

The input output configuration, number of logic elements and injected fault sets in circuit given in Table I. Fault model used in proposed method is stuck fault model. We choose other medium c880 (8 bit ALU) and large c7552 (32 bit adder cum comparator) benchmark circuits to validate proposed design.

B. Power Analysis

There are two modes of operations in Scan based BIST circuitry, test mode and normal mode. The power consumption due to test application time may give rise to severe hazards to the circuit reliability, maintainability and availability. Hence it is an important aspect to optimize power during testing. In VLSI, according to thumb rule 50% of the total integrated circuits cost is due to testing, the Moore’s law explains the fabrication cost of transistor decreases over decades but testing cost is constant. In our research we are more concern with dynamic power because static power can be neglected because it is due by leakage currents when the gates are operating in the idle mode.

C. Dynamic power dissipation

Dynamic power dissipation is primarily caused by the current flow from the charging and discharging of parasitic capacitances. It consists of three components: switching power, glitch power and short-circuit power. In most CMOS digital circuits, the switching power is the most important part in power dissipation. The power dissipation is equivalent to the energy required to charge the output node to and discharge the total output load capacitance to ground (GND). The generalized expression for the power dissipation of a CMOS logic gate can be calculated from the equation 1.

$$P = \alpha T \cdot C_{load} \cdot V_{DD}^2 \cdot f_{clk}$$  \hspace{1cm} (1)

Here switching or transition activity is $\alpha T$. The total load capacitance is represented by $C_{load}$. The supply voltage is given by $V_{DD}$ and the operating frequency is represented by $f_{clk}$, the dynamic power is directly proportional to the transition activity factor of the gate $\alpha T$.

![Figure 1: Basic Testing Principle](image1)

![Figure 2: Combinational circuit with Scan flip flop](image2)

![Figure 3: Full scan design](image3)

<table>
<thead>
<tr>
<th>Benchmark circuit</th>
<th>PIs</th>
<th>Pos</th>
<th>Number of gates</th>
<th>Equivalent fault set</th>
<th>Fault type</th>
</tr>
</thead>
<tbody>
<tr>
<td>C432</td>
<td>36</td>
<td>7</td>
<td>160</td>
<td>1078</td>
<td>${s_a_0, s_a_1}$</td>
</tr>
<tr>
<td>C880</td>
<td>60</td>
<td>28</td>
<td>794</td>
<td>1884</td>
<td>${s_a_0, s_a_1}$</td>
</tr>
<tr>
<td>C7552</td>
<td>207</td>
<td>108</td>
<td>3513</td>
<td>15100</td>
<td>${s_a_0, s_a_1}$</td>
</tr>
</tbody>
</table>
The power results are obtained from the Xilinx 14.5 implementation with the device XC3S1200E targeted on Spartan 3E in which we have generated and added input files after the post simulation. X power analyzer tool used for the Power analysis, this analyzer takes certain input files viz .ncd file, pcf file and vcd file for analysis.

D. Transition Activity

Transition activity represents the transitions in the bits of the input test vector. It is essential for measuring power in digital circuits, the total power consumption of a circuit during test by reducing the transitions among patterns. The transitions are reduced in two dimensions one is between consecutive patterns used to test combinational circuit, for example test vectors:

\[ T_1 = 10111 \quad TA = 2 \]
\[ T_2 = 10110 \quad TA = 3 \]

and second is between consecutive bits used in sequential circuit, for example test vectors:

\[ T_2 = 10111 \]
\[ T_2 = 11110 \quad TA = 2 \]

The proposed scheme is evaluated using industrial benchmark circuit c432. This can be illustrated by implementing the LFSR, Bitswapping and SIC LFSR for \( N=5 \) bit. For a 5 bit LFSR the primitive polynomial equation is given by \( X^5+X^3+1 \). The external-XOR LFSR with the above data is given figure 4.

![Standard 3 bit LFSR](image)

The transition activity (TA) obtained by implementing the 5 bit LFSR is shown in table II. The response of transition activity based on the bit position i.e. how the switching transitions are taking place at each bit position is also shown in table III. The output TA for the LFSR, BS and Efficient SIC LFSR are observed and the total transitions are demonstrated at every clock cycle which is represented in table IV, where X-filling techniques used for power aware and test time applications, in proposed approach zero fill, fill in don’t care bits with logic 0 and one fill, fill in don’t care bits with logic 1.

<table>
<thead>
<tr>
<th>N</th>
<th>LFSR</th>
<th>BS</th>
<th>Saving (%)</th>
<th>SIC – LFSR with X filling</th>
<th>Saving (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>80</td>
<td>64</td>
<td>20</td>
<td>31</td>
<td>61.25</td>
</tr>
</tbody>
</table>

Table II. Switching Activity

Table III. Bit wise switching activity

<table>
<thead>
<tr>
<th>Clk</th>
<th>Bit Swapping LFSR</th>
<th>One Fill</th>
<th>Zero Fill</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>11111</td>
<td>11111</td>
<td>00000</td>
</tr>
<tr>
<td>1</td>
<td>01111</td>
<td>11110</td>
<td>00001</td>
</tr>
<tr>
<td>2</td>
<td>00111</td>
<td>11100</td>
<td>00011</td>
</tr>
<tr>
<td>3</td>
<td>00011</td>
<td>11010</td>
<td>00010</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>26</td>
<td>00110</td>
<td>01000</td>
<td>10011</td>
</tr>
<tr>
<td>27</td>
<td>10011</td>
<td>01011</td>
<td>10010</td>
</tr>
<tr>
<td>28</td>
<td>11001</td>
<td>01101</td>
<td>10110</td>
</tr>
<tr>
<td>29</td>
<td>11010</td>
<td>01100</td>
<td>10111</td>
</tr>
<tr>
<td>30</td>
<td>11110</td>
<td>01110</td>
<td>10101</td>
</tr>
<tr>
<td>31</td>
<td>11111</td>
<td>01111</td>
<td>10100</td>
</tr>
</tbody>
</table>

Transitions = 64 Transitions = 31 Transitions = 32

Table IV. Clock wise Transition Activity comparison

III. HARDWARE IMPLEMENTATION

A. Hardware Implementation using X-filling technique

The SIC generator is very efficient for combinational, sequential and memory testing for single and multiple stuck faults and delay faults. The \( n \) bit binary SIC generator can be constructed using \( n \) bit binary counter, used to generate deterministic patterns which are unable to detect stuck at faults to overcome this problem a phase shifter circuit is added to counter, phase shifter comprises of XOR gates used to generate single input change pairs, which is the most widely used test pattern generator because of its small circuit area overhead and excellent pseudo random characteristics as shown in figure 5. X-filling techniques are widely used in TPG as seed generator, because of its pre selected option and excellent random behavior, in [2]. Modified LFSR is used as the seed generator, which increase area and power of the circuit, the novelty of proposed SG replace with zero fill and one fill value to generate low power test patterns as shown in Fig. 6, the proposed architecture which is called Efficient SIC X-filling generator. The counter and SG are controlled by test clock CLK.
For example \( N = [4:0] \)

\[
\begin{align*}
\{ C[0], C[1], C[2], C[3], C[4] \} &= \{ 1 \ 1 \ 1 \ 1 \ 1 \} \\
\{ S[0], S[1], S[2], S[3], S[4] \} &= \{ 1 \ 0 \ 0 \ 0 \ 0 \}
\end{align*}
\]

A shifter circuit shown in Fig. 3 is used to encode the counter’s output \( C[n-1:0] \) so that two successive values of its output \( S[s-1:0] \) will differ in only one bit. Phase shifter is implemented as follows.

\[
\begin{align*}
S[0] &= C[0] \oplus C[1] \\
\vdots \\
S[N-1] &= C[N-1] \oplus C[N-1]
\end{align*}
\]

For example \( S \{ 0 \ 0 \ 0 \ 0 \ 1 , \ 0 \ 0 \ 0 \ 1 \ 1 , \ 1 \ 1 \ 1 \ 1 \ 0 , \ldots \ldots \} \)

The proposed architecture shown in figure 6 called Efficient SIC Generator comprises of a SIC generator and Seed Generator. The input to XOR gate is a non zero seed value from BS circuit, it is a modified LFSR with 2:1 Multiplexer structure, to obtain minimal switching, the swapping between the neighboring bits is required as proposed in [11-15], the swapping process as follows if the last bit (selection line) is “0”, then swapping is performed, else nothing will change. The final test vectors are obtained as shown below equations:

\[
\begin{align*}
PG[0] &= SG[0] \oplus S[0] \\
\vdots \\
PG[N-1] &= SG[N-1] \oplus S[n-1]
\end{align*}
\]

Here Pattern generator (PG) bits obtained by XOR operation between bit 5-bit SIC generator output sequence and non zero seed value from SG are \{11111, 11110, 11100, 11101, 01101, 01110, 01111 \ldots \ldots \}. The preselected zero fill and one fill seeds SG is \{00000\} and \{11111\} will be xor-ed with sequence:

\{11000,11001,11011,11010,11110,11111,11101,10000 \} and generates the \( p[n-1:0] \) applied to scan chain. \{11100, 11101,11111,11110,11010,11011,11001,10100\}.

IV. RESULT ANALYSIS

To validate the efficiency of the proposed approaches, we select pattern generators LFSR [2], LSA TPG [2], Bipartite LFSR [2] and LP-LFSR [3]. Power analysis comparison with [1] has shown in below tables. Simulation and synthesis were carried out for functional verification.

### TABLE V. POWER CONSUMED BY CUT

<table>
<thead>
<tr>
<th>TPG</th>
<th>LFSR[2]</th>
<th>Proposed</th>
<th>Saving (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumed (mw)</td>
<td>1.629</td>
<td>0.56</td>
<td>65.62</td>
</tr>
</tbody>
</table>

The test patterns generated from this SIC X-filling LFSR is tested with ISCAS Benchmark Circuit C432, it is verified that the proposed method gives dynamic power reduction 0.56 mw and 0.101 mw compared to the conventional methods.

### TABLE VI. POWER CONSUMED BY CUT

<table>
<thead>
<tr>
<th>TPG</th>
<th>LSA-TPG [2]</th>
<th>Proposed</th>
<th>Saving (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumed (mw)</td>
<td>0.188</td>
<td>0.101</td>
<td>46.80</td>
</tr>
</tbody>
</table>
The variations of bit patterns generated by X-filling techniques shown in figure 7, X axis gives clock period and Y axis describes the decimal equivalent of the generated patterns. The generated patterns applied to CUT C432 using Fastscan Tessent Tool, a statistics report shown in table VIII.

TABLE VII. STATISTICS REPORT

<table>
<thead>
<tr>
<th>Statistics Report</th>
<th>Stuck-at Faults</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fault Classes</td>
<td>Faults (total)</td>
</tr>
<tr>
<td>FU (full)</td>
<td>1078</td>
</tr>
<tr>
<td>DS (det_simulation)</td>
<td>1065 (98.79%)</td>
</tr>
<tr>
<td>RE (redundant)</td>
<td>13 (1.21%)</td>
</tr>
<tr>
<td>Coverage</td>
<td></td>
</tr>
<tr>
<td>Test_coverage</td>
<td>100.00%</td>
</tr>
<tr>
<td>Fault_coverage</td>
<td>98.79%</td>
</tr>
<tr>
<td>atpg_effectiveness</td>
<td>100.00%</td>
</tr>
<tr>
<td>Test_patterns</td>
<td>63</td>
</tr>
<tr>
<td>Simulated_patterns</td>
<td>80</td>
</tr>
<tr>
<td>CPU time (secs)</td>
<td>1.4</td>
</tr>
</tbody>
</table>

V. CONCLUSION

An SIC X-filling generator is a low power and high fault coverage test pattern generator has been proposed in which the filling techniques are used in which seed values Xored with the single input change (SIC) generator. This method adequately and effectively reduces the switching correlations among the test patterns and achieved high fault coverage in minimum pattern length compared to the existing methods. The drawback of proposed method is area overhead; it can be overcome by increasing speed of the generator without effecting length of bits and technology library. It is verified from the results that power reduced by the proposed method is 65.62% and 46.80% with respect to DUT.

REFERENCES