A Digital Sweep (Chirp) Generator With Extremely Small Memory Size And High Level Of The Spurious Free Dynamic Range

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***Abstract* - This paper presents an efficient technique to extremely increase the performance of Pedersen's digital chirp generator concerning the level of the Spurious-Free Dynamic Range (SFDR) and size of the memory. The proposed digital chirp generator uses the piecewise parabolic interpolation to decrease the memory size and system complexity while maintaining excellent spectral performance in comparison with the other techniques.**

Keywords: Coherent digital chirp generator, Direct digital frequency synthesizer, Piecewise parabolic interpolation.

I. INTRODUCTION

Several applications require coherent sweep (chirp) signals, i.e. a sweep where both the phase and frequency must be specified for all time. Examples of such applications are target velocity estimation [1], phase coding of sweep signals in communication applications, system characterization, radar, especially in Synthetic Aperture Radar (SAR), sonar, acoustic digital imaging, and the determination of system response with network analyzers [2].

A method for the generation of digital chirp signals was proposed by Pedersen [3]. His approach is based on the real time digital evaluation of the phase of the desired sweep signal and then reads its value from a look-up-table (LUT) of length L ($L = 2^K$). The main disadvantage of Pedersen's chirp is the high level of spurious harmonic distortion [4, 5]. A chirp generator was reported in [6], in which the fractional bits are utilized to interpolate the sample values that are not stored in the LUT and in this way increases the effective LUT length. This technique is known as fractional addressing and was utilized to reduce the level of spurious harmonic distortion. Another chirp generator in which fractional addressing is utilized, was reported in [7]. The major disadvantage of the digital chirp generator in [7] is that it requires the implementation of two independent chirp generators and in order to evaluate the phase difference between the two generated chirp signals. The hardware requirements, therefore, make its implementation costly.

Efficient LUT compression techniques were reported in [8, 9] and utilized to improve the performance of a Direct Digital Frequency Synthesizer (DDFS). This technique will be used to obtain the new digital chirp (chirp) generators. The digital chirp generator is expected to have the lowest memory size and the highest spurious-free dynamic range (SFDR) in comparison with the previous techniques.

On these bases, this paper presents a detailed analysis of coherent digital chirp generator using the methodology of the piecewise parabolic interpolation.

In section 2 we briefly describe DDFS and the efficient compression technique, which is based on the methodology of the piecewise parabolic interpolation. In § 3 reported the methodology of the Pedersen's chirp generator. The proposed digital sweep (chirp) generator is described in § 4 and this section shows the improvement on Pedersen's chirp generator using the piecewise parabolic interpolation. The simulation's results and conclusions will be shown in sections 5 and 6, respectively.

II. DIRECT DIGITAL FREQUENCY SYNTHESIZER (DDFS) AND THE PIECEWISE PARABOLIC INTERPOLATION TECHNIQUE

A. Introduction to DDFS

Direct digital frequency synthesizers (DDFSs) are able to generate single phase or quadrature sinusoids with excellent frequency resolution, good spectral purity and phase continuity on switching [10]. DDFS plays an important role, both in modern communication systems and in measurement instrumentation. In the next section, simple modifications will be applied to the phase-generation circuitry in order to produce synthesized chirps, which are useful in (SAR) and in many applications.

The basic DDFS architecture was introduced in [11]. DDFS synthesizes a sine wave by using a periodically overflowing phase accumulator to generate and store the phase information, DDFS also uses a ROM based look up table to compute the sine function, as shown in figure 1, where the frequency of the generated sine wave is controlled by the Frequency Input Word (FIW).

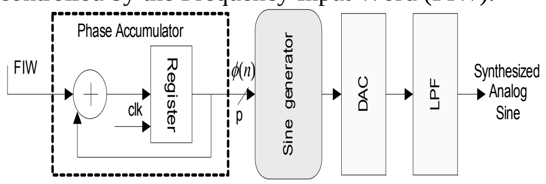

Figure 1: DDFS Architecture

Equation (1) presents the frequency relations of a DDFS structure.

$$f_{\min} = \frac{f_{clk}}{2^L}$$
$$f_{out} = f_{\min}.FIW \qquad 0 \le FIW \le 2^{L-1} \quad (1)$$

where $f_{\min}$ is the minimum synthesizable frequency, f_{clk} is the clock frequency, L is the word length of the phase accumulator, f_{out} is the output frequency, FIW is the frequency input control word.

The most critical block in DDFS is the sine generator, which limits the maximum operating frequency of the system and it is responsible for most of the DDFS power consumption. The common approach to simplify the sine generator exploits the quadrant symmetry of trigonometric functions and identities. For a quadrature DDFS, this reduces the task of the sine generator to the calculation of sine and cosine functions for angles belonging to $[0, \pi/2]$ interval only. For single-phase DDFS, sine calculation for phase angle belonging to the first quadrant is required. Piecewise-Polynomial approximation for the sine generator is proposed in [8] to use it in the new chirp (chirp) generators. This approach gives the maximum SFDR in comparison with the other techniques in the literature.

B. Piecewise-Polynomial DDFS

DDFS is inherently as frequency stable as the reference clock. It provides numerically highly linear frequency tuning with controllable frequency resolution. A simple implementation of DDFS uses a ROM lookup table to calculate the trigonometric functions. Unfortunately, in spite of memory saving, due to both of the phase truncation and quadrant symmetry, a large lookup tables are needed because they slow down the DDFS' operations and increase the power consumption. Hence, many ROM compression techniques [12-14] aimed to reduce the lookup table size, since the straight forward implementation of the sine function look-up table requires more than 4 Giga samples of storage for a phase accumulator resolution of 32 bits and output resolution of 12 bits.

Eltawil and Babak [8] and De Caro [9] proposed an architecture, which employs a second and higher order interpolations functions to further compress the ROM size, while maintaining or exceeding the spectral purity of the techniques mentioned above, with minimal hardware overhead. Eltawil's architecture depends on a piecewise parabolic Farrow structure [15] due to its hardware efficient implementation and good performance.

The fundamental equation for digital interpolation of data signals is as follows:

$$y(kT_i) = y[(m_k + \mu_k)T_s] = \sum_{i=I_1}^{I_2} x[(m_k - i)T_s]\, h_I[(i+\mu_k)T_s] \quad (2)$$

where $\{x(m)\}$ is a sequence of signal samples taken at interval T_s, μ_k is a fractional shift, m_k is the base point index, and $h_I(t)$ is a finite-duration impulse response of a continuous time analog interpolating filter as it is shown in (3). The Farrow implementation assumes that the impulse response is a piecewise defined polynomial in each T_s segment (section) with $i \in [I_1, I_2]$.

$$h_I(t) = h_I[(i+\mu_k)T_s] = \sum_{n=0}^{N} b_n(i)\mu_k^n \quad (3)$$

The coefficients $b_n(i)$ are fixed numbers, independent of μ_k, determined by the filter's impulse response $h_I(t)$. These coefficients are chosen to provide the widest pass-band and the strongest attenuation at multiples of the sampling frequency. We can consider $y(kT_i) = y(k)$, after we substitute (3) in (2) and rearrange terms to show that the interpolation can be performed by (4).

Technically, the sine wave is divided into four basic quadrants; each quadrant is subdivided into sections. By exploiting the symmetry of the sine/cosine wave, only the parameters that are relevant to one quadrant need to be stored, instead of storing values of the sine function directly in the ROM as in the traditional methods, the interpolation coefficients will be stored. The Farrow structure as in [15] receives input samples from the sine wave and performs the interpolation based on the neighboring three points. Thus, for each base point (sample of the sine), three interpolation coefficients are computed. These interpolation coefficients are used according to (4) in order to compute the value of the sine wave at any arbitrary fractional delay specified by μ_k.

$$\begin{aligned} y(k) &= \sum_{i=I_1}^{I_2} x(m_k - i) \sum_{n=0}^{N} b_n(i)\mu_k^n \\ &= \sum_{n=0}^{N} \mu_k^n \sum_{i=I_1}^{I_2} b_n(i) x(m_k - i) \\ &= \sum_{n=0}^{N} \mu_k^n v(n),\ v(n) = \sum_{i=I_1}^{I_2} b_n(i) x(m_k - i) \end{aligned} \quad (4)$$

For parabolic interpolation we have:

$$y(k) = V_1(2) + \mu_k V_2(2) + \mu_k{}^2 V_3(2) \quad (5)$$

where μ_k is the fractional shift, n is the base point index and k is the fractional delay index. The interpolation calculation has been pre-computed for a specified number of base points (sections) of the sine wave and stored in a ROM. Each word in the ROM consists of (V_1, V_2, V_3) which in conjunction with the fractional delay μ_k can be used to calculate intermediate points between two base points [8].

III. PEDERSEN'S DIGITAL CHIRP GENERATOR

The digital generation of coherent digital sweep signals (Pedersen, 1990) is based on performing the generation of the phase of a linearly swept signal in real-time, then it implements the extraction of $\mathrm{mod}(2\pi)$ from the total phase, and then generates the desired sine or cosine swept signals by means of a look-up-table. Let $w(t)$ be the instantaneous frequency of a linearly swept signal with start frequency of w_1 and sweep rate of S (Hz/s). $w(t)$ is given as:

$$w(t) = 2\pi St + w_1 \quad (6)$$

The corresponding instantaneous phase is obtained by integrating (6):

$$\phi(t) = \pi St^2 + w_1 t + \phi_0 \quad (7)$$

where ϕ_0 is the initial phase, the linear term provides the constant frequency offset (zero for a base band signal) the quadratic term in (7) corresponds to the linearly varying frequency. The generation of the coherent digital chirp signal is started by double integration for the constant sweep rate in the time domain to obtain (6) and (7), then the extraction of mod (2π) from the total phase, and after that the generation of the desired sine or cosine swept signals by means of the look-up-table. This is illustrated in figure 2. The main disadvantages of Pedersen's chirp generator are the high level of spurious harmonic distortion and the large memory size. The actual digital implementation for figure 2 is illustrated in figure 3.

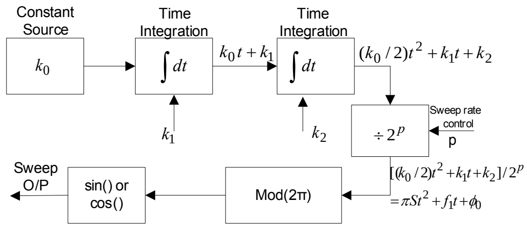

Figure 2: Functional block diagram of the Digital Chirp Generator

The two integrations are performed by means of a counter and an accumulator. Choosing address lines that contain the more significant bits of the accumulator output lines will produce a low sweep rate while output lines containing the less significant bits will result in a higher sweep rate. This approach is well documented in [3].

The address size, k of the sine LUT determines the accuracy of the phase data to the LUT. Of course k cannot exceed the size of the accumulator, and the k bits typically constitute only a small fraction of the total number of accumulator output lines. The selection of the k bits used as address lines is defined
by the parameter, p as illustrated in figure 4 , where p is

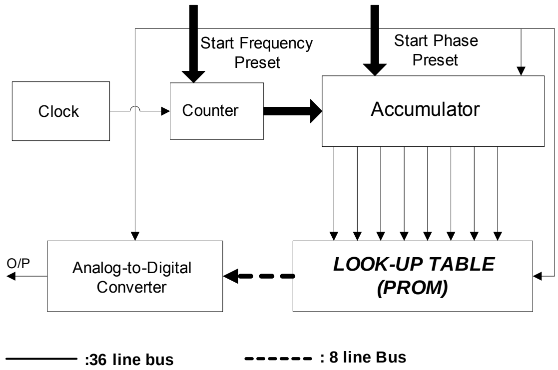

Figure 3: Block diagram of the Pedersen chirp generator

the position of the least significant bit of the accumulator output which is used as an address line into the LUT. The smallest value that p can assume is $p = 0$. The k input lines into the sine LUT are the bits $[p, p+1, p+2, ..., p+k-1]$. Since the k input lines are shifted to the left by p bits, relative to the least significant bit of the accumulator.

The unused accumulator bits $[0, 1, 2, ..., p-1]$ represent accuracy that is not utilized. As seen and illustrated in figure 4 below, the bits $[p+k,\ p+k+1,\ p+k+2, ..., n-1]$ are not used either. These bits represent a count of the number of completed cycles which is unrelated to the signal generation.

The sine (or cosine) LUT is of the size $2^k \times q$ where q is the number of bits used to represent the sine or cosine data in the PROM table.

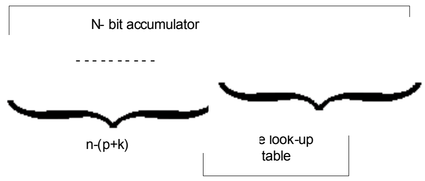

Figure 4: Definition of the output lines from the accumulator

IV. THE IMPROVED DIGITAL CHIRP GENERATOR

The proposed system is a hybrid of the digital chirp generator and the system using interpolation based direct digital frequency synthesis. The interpolator uses predetermined interpolation coefficients to fit the sine wave from the calculated phase instead of using a predetermined waveform stored in a big sized memory. This implies that a smaller look-up table for the sine function is used compared to existing architectures with a minimum overhead hardware, and it is expected to have higher SFDR than the previous methods. Thus only the interpolation coefficients are stored in the memory. Figure 5 shows the block diagram of the proposed chirp generator.

The frequency of the clock in figure 5 determines the highest frequency that the digital chirp can generate.

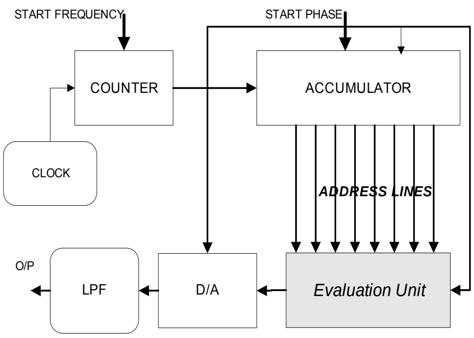

Figure 5: Block diagram of the implementation of Pedersen digital chirp generator

In this chirp generator the start and end frequency can be controlled by the initial content of the counter and the accumulator. Furthermore, the sweep rate can also be controlled by the location and size of the address lines. The coherent digital chirp generator uses the clock to trigger the counter (first integrator) and feeds the output to the accumulator (second integrator). In general, the phase of the sweep signal is not equal to the value of the phase stored in the accumulator because only a subset k of the output lines from the accumulator is sent to the look-up table.

Al-Ibrahim in [16] presented an efficient architecture with low level spurious harmonic distortion. The drawback of his architecture is inherited in the relatively large size of its ROM and the complexity of the implementation. On the other hand our architecture accomplishes the generation for the coherent digital sweep signals, with low level of the spurious harmonic distortion, low cost in complexity, and smaller size of ROM.

The new architecture uses the Farrow structure [15] to generate the interpolation coefficients. The output of this interpolation based chirp generator is comparable with other methods that implement the look-up table method. Alternatively, the size of the ROM is reduced by a factor of more than 128 times with respect to the one in Pedersen's approach, when using 12 address lines and 15 bits word size. Then again, we increase the performance of our architecture by using a higher order interpolation instead of using a second order interpolation only. This is easily controllable by our Matlab simulation. As we will see later when we increase the number of interpolation coefficients the error will be decreased further. Equation (8) is a polynomial equation derived from (5); it is for cubic and higher order interpolations:

$$y(n,k) = V_1(n) + \mu_k V_2(n) + \mu_k{}^2 V_3(n) + \mu_k{}^3 V_4(n) + \dots \quad (8)$$

where μ_k is the fractional shift, n is the base point index, and k is the fractional delay index.

Regarding to this equation, the simulated structure generates four interpolation coefficients for each section, for example if we divided the quarter of the sine wave to three sections, we will get 3x4=12 interpolation coefficients, etc. Based on (8), our implementation improves the system which was reported in [3] to decrease the error and the spurious harmonic distortion; this is done when we increase a quadratic equation to become a cubic equation. Consequently, four interpolation coefficients will be generated and appear instead of three coefficients.

V. SIMULATION RESULTS

The simulations were conducted by simulating figure 5 within figure 6 to realize the polynomial evaluation unit. Figure 7 shows the generated chirp signal based on the proposed method.

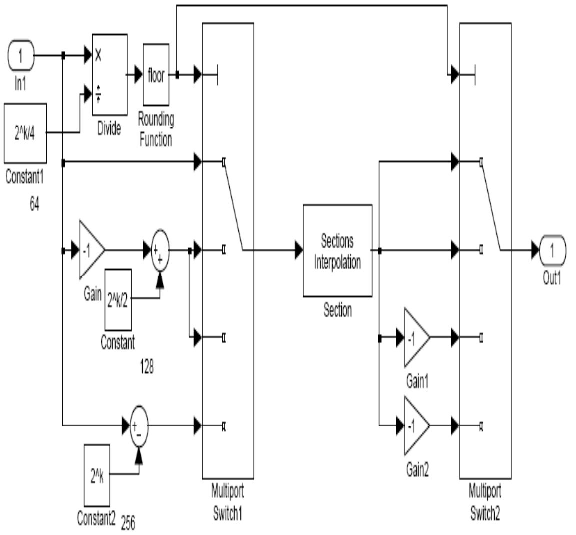

Figure 6: The block diagram of the simulated structure works instead of Farrow structure to generate the sine wave.

Samarah and Loffeld [17] showed the measurements of the spectral purity and the comparison between this technique and the other techniques in the literature with respect to the spurious free dynamic range (SFDR) and it shows that the proposed technique is much better than the others.

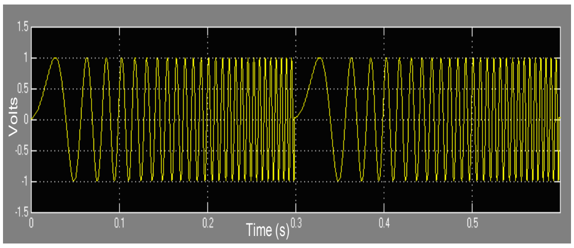

Figure 7: The generated coherent swept signal by the new technique (2 periods)

Assuming that the minimum number of samples required determining one cycle of the waveform is 5, and a maximum frequency 10 MHz is needed, the clock frequency needs to be at least 50 MHz. we consider that the 8 least significant bits from the accumulator have been chosen as the address lines to the LUT memory (Evaluation unit). This encoded 8-bit output can have values from 0 to 255 and is defined to represent a phase between 0 and 2π radians where 0 corresponds to 0 radian and 255 corresponds to $(255/256)\times 2\pi$ radians.

Figure 8 shows the spectrum of the sweep signal using Pedersen's method, while figure 9 illustrates the spectrum of the chirp signal using piecewise parabolic interpolation with 16 segments per quadrant (proposed method). These figures show the efficiency of the interpolation technique. While figure 10, figure 11**,** and Fig.12 show how the order of the interpolation equation and the number of sections important are.

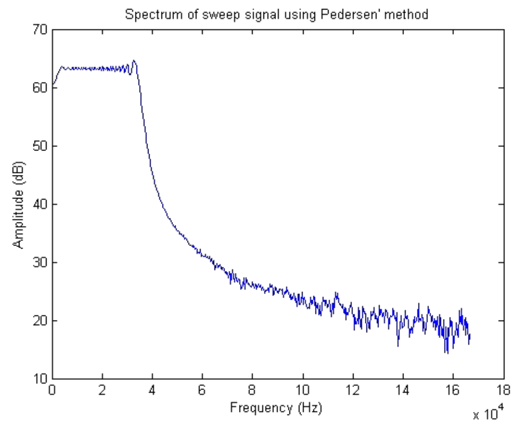

Figure 8: Output spectrum of chirp signal using Pedersen's method

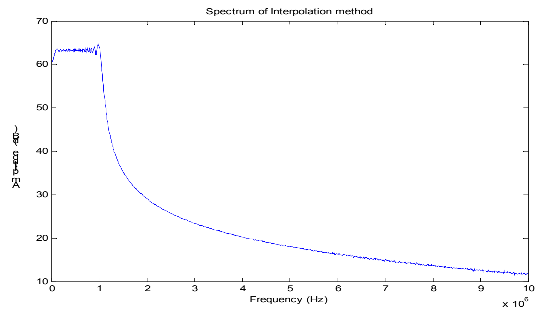

Figure 9: Spectrum of chirp signal using the interpolation method (Order=2, segments=16)

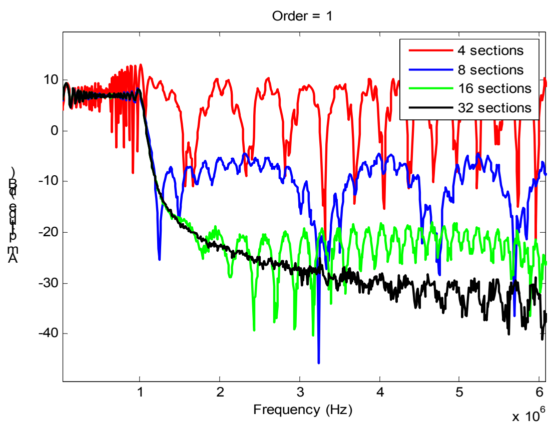

Figure 10: The spectra of the chirp signal with order=1 and different number of sections/quadrant

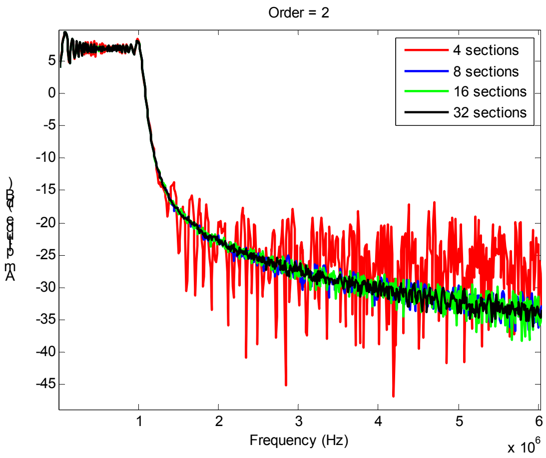

Figure 11: The spectra of the chirp signal with order=2 and different number of sections/quadrant

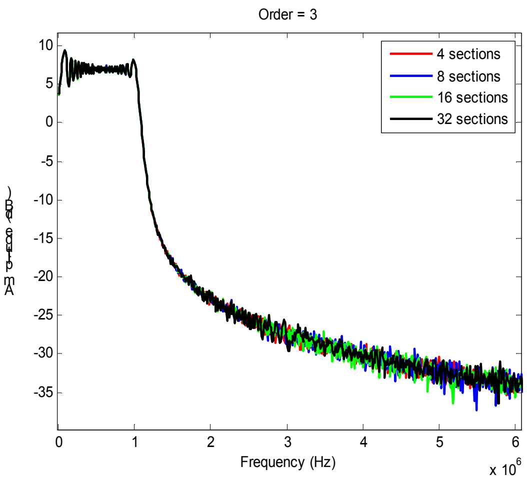

Figure 12: The spectra of the chirp signal with order=3 and different number of sections/quadrant

For instance, when we increase the number of segments (sections) and the order of the interpolation equation, the error will be decreased.

VI. CONCLUSIONS

A novel technique was proposed to generate sinusoidal waves based on a piecewise-polynomial approximation. The proposed sweep (chirp) generator shows an extremely high level of the Spurious Free Dynamic Range (SFDR) reaches 97,5 dBc and at the same time reduces both the hardware complexity and memory size of the LUT.

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