Voltage Controlled Delay Line Applied with Memristor in Delay Locked Loop

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Abstract—In this work, one of memristor characteristic; the varying resistance is applied in CMOS integrated circuits alongside the transistors. Due to memristor small size, by merging memristor and CMOS circuit elements can probably save up area consumption and thus overcome scale limitation problem. In this paper, a delay locked loop has been designed using voltage controlled delay line that was used together with a memristor. By adjusting the resistance of memristor, it was possible to control the bias voltage to get different delays of a single unit delay. In regards to whole DLL designs, we choose phase-frequency-detector (PFD) for phase detector and charge pump with capacitor for the loop filter. The designs are explained including its operation method and considerations on speed and power consumption. Finally, the simulations result of the DLL with varying resistance of memristor will also be discussed. The DLL is designed using 0.18um process.

Keywords—memristor, memristor model, memristor switching behavior, delay-locked-loop, phase-frequency detector, charge pump

I. INTRODUCTION

The first physical realization and understanding of the memristor switching mechanism was reported by Stan William and his group from HP lab [1], [2]. Since the memristor discovery, researchers and engineering professionals have been trying to understand the new device and develop potential applications of memristor. Among memristor application fields are shown in Figure 1. Memristor offers non-volatile memory device [3, 4] with high density and speed as fast as DRAM. The switching ability of ON state and OFF state brings up memristor potential in logic circuit [5] where the logical states represented as resistance. In neuromorphic system, memristor mimics the role of synapses, such that each device may interact with other devices throughout the system [6].

Another promising memristor application is implementation in analog circuit as a programmable resistor. According to Leon Chua, a mathematician who first proposed the idea of memristor in [7], memristor is a resistor, with varying resistance, where the resistance changes according to the total amount of charge that flow through its entire history. Since memristor resistance changes according to supply voltage, memristor is used in programmable analog circuits as proposed in work [8]. They built several programmable analog circuits demonstrating memristor based programming of threshold, gain and frequency. Another example of memristor-based programmable resistance is proposed in work [9] where fine resolution programmable memristance is achieved by varying the amount of charges flowing or flux across the memristor. The programmable resistance memristor is used as programmable gain amplifier.

In this work, we try to apply memristor as variable resistor in CMOS integrated circuits in order to reduce area consumption since memristor is much smaller than transistor size (only 15 to 30 nm according to William physical model for a single memristor). We apply a memristor in voltage controlled delay line of the delay locked loop where the resistance is adjusted to control the delay of the delay line.

This paper is divided into 5 sessions including the introduction and conclusion. Session 2 will emphasize on delay locked loop block designs which are the phase detector and charge pump and explanation of the proposed voltage controlled delay line with memristor. Session 3 briefly explained on basic information of memristor structure and its behavior. Next, the simulation results of DLL using VCDL with memristor is shown and discussed in session 4.

Figure 1: Among memristor applications in recent researches
II. DELAY LOCKED LOOP

A conventional analog DLL consists of several blocks which are phase detector, charge pump, low pass filter and voltage controlled delay line. The block diagram is shown in Figure 2. Here, the DLL adjusts the delay of the delay line until the inputs to the phase detector are in phase.

A. Phase Detector

A phase detector generates an output signal which is proportional to phase difference between its two input signals. The typically used phase detectors are made from digital components and common examples of phase detectors are XOR, flip-flop and phase-frequency detector (PFD). In this work, we choose the PFD design for its simplicity, low power and high speed [10]. There are two input signals to PFD; clock reference which may come from system clock or the processor clock (clkref) and clock from delay line (clkdel). The PFD generates two outputs called the UP and DOWN signals. A conventional PFD consists of two D-type flip-flops (DFF) and simple AND gate is shown in figure 3.

Here, the D-input for both flip-flops are wired high. Based on the truth table, when clkref is rising and D is high, the next Q output will be high, thus resulting in changing the UP signal to high. This continues as long clkdel is zero. Next, when clkdel is rising, the DOWN signal also changing to high. At this point, both the inputs of AND gate are high thus turning on reset signal for each flip flops making both output turn low. The length time between rising edge of clkref and clkdel is actually phase difference between both input signals. When clkref leads clkdel, the average value of UP signal will be proportional to the phase difference and DOWN signal will be zero. Otherwise, when clkref lags clkdel the average value of DOWN signal reports the phase difference and UP signal will be zero. When the inputs are in same phase, both outputs are low. Figure 4 shows the schematic of PFD where the DFF is implemented using True Single Phase Clock (TSPC) design, a faster and simpler logic circuit for higher speed and low power phase detector.

B. Charge Pump and Low Pass Filter

A charge pump generates control voltage for delay line in accordance to output signal from PFD. This control voltage adjusted delay for delay line thus reducing the phase difference. Basically, charge pump consists of two current sources and transistors to act as switches. The switches will control current to flow into or out from the capacitor. The block diagram is shown in figure 5. The capacitor is the low pass filter which integrates the charge pump output current to an equivalent control voltage (Vcntl). The UP signal is connected to switch that allows current to flow into capacitor thus charging up control voltage whereas the down signal is connected to switch that allows current flowing out from capacitor thus voltage is discharge to ground. When both reference clock and delay clock is in same phase, the PFD will generate no UP or DOWN signal thus no current will flow into or out from the capacitor. The operations are summarized in table 1. Figure 6 shows the schematic of charge pump with capacitor. The current source is built up using bias circuit.
C. Voltage Controlled Delay Line With Memristor in DLL

Figure 7 shows block diagrams of the voltage controlled delay line with memristor used in the DLL. Proposed design uses a current starved as shown in Figure 8. Here, the inverter delay is determined by the size of load capacitance and amount of (dis)charging current. To apply a current starved inverter as controllable delay element, we control the gate voltage of M1 and M2 where transistor M1 control the rising edge of input signal and transistor M2 is otherwise. In other words, we control the (dis)charging current of the output parasitic capacitor C of middle inverter, thus regulate the propagation delay of this element. Therefore, by adjusting the resistance of memristor, we control the bias voltage for current starved inverter to get different delays.

Assuming circuit in saturation region, we can get the $I_{DS}$ for particular $V_{ctrl}$.

$$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{Vctrl} - V_{TH})^2 \quad (1)$$

From equation (1) we can determine the delay of the delay element. If the delay line using $N$ numbers of delay element, thus total delays from delay line will be $N \times t_{delay}$.

$$t_{delay} = C_{load} \frac{V_{IN}}{I_{DS}} \quad (2)$$

For demonstration purpose, we adopted the memristor SPICE model from [1] to get sample of memristor resistance range. The resistance is derived from voltage divides over current. Figure 10 shows resistance of memristor SPICE model in positive voltage supply only. When voltage increase from 0V to 1V in (a), the oxygen vacancies in the doped TiO$_{2-x}$ layer are repelled, moving them towards the undoped TiO$_2$ layer. As a result, the boundary between the two materials moves, causing an increase in the percentage...
of the conducting TiO$_{2-x}$ layer thus the resistance decreases. When voltage decreases from 1V to 0V in (b), the oxygen vacancies still moving since there is voltage supply, but with slower speed and resistance decreases steadily. This is how a memristor can have variable resistance while changing the supply voltages.

Figure 10. Resistance of memristor SPICE model in [1]

IV. RESULTS AND DISCUSSIONS

Using the sample resistance range, we run simulations using Mentorgraphics in 0.18um process by varying the resistor value from 4kΩ ($R_{ON}$) to 11kΩ ($R_{OFF}$). The result is shown in Figure 11. In Figure 10 (a) when clkref leads clkdel, UP signal is generated thus current is flowing to capacitor thus increase Vc. Otherwise, in Figure 10 (b) when clkref lags clkdel, DOWN signal is generated thus current is flowing out from capacitor thus Vc is discharged to ground. At this point, as we increase the resistance, Vctrl is decreasing thus $I_{DSS}$ is decreasing results in smaller delays or otherwise.

A DLL requires large operating frequency range in order to meet various products specifications. However, as reported in [11], the highest operating frequency of a DLL is limited by the minimal delay of a single delay unit while the lowest operating frequency is restricted by the length of delay line. In order to meet the maximum and the minimum speed requirement at the same time, DLL demands a delay line composed of delay units with very minimal delay. However, this will require very long delay line which cause in large DLL area consumption.

Total delay of delay line ($T_{DEL}$) = Number of delay unit (N) x Delay of single delay unit ($t_{del}$)

By applying memristor to voltage controlled delay line, we increase the resistance of memristor, thus decrease current that control delay of single delay unit as shown in equation 2. Therefore, we can expand total delay of the delay line until maximum resistance. This is how we maximize operating frequency range without adding up more delay units.

Figure 11. Simulation result for (a) clkref leads clkdel and (b) clkref lags clkdel for input frequency 1GHz and resistance from 4kΩ to 11kΩ

V. CONCLUSION

In this paper, delay locked loop has been designed using voltage controlled delay line that was used together with a memristor. By adjusting the resistance of memristor, it was possible to control the bias voltage to get different delays of a single unit delay. This paper covers only on the conceptual idea of applying memristor in an analog circuit which is DLL. In future, research will be conducted to determine how to control the memristor resistance and interfacing the memristor with CMOS circuit.

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