Integrated High Speed Current-Mode Frequency Divider With Inductive Peaking Structure

Hyeim Jeong
School of ECE, Chung-buk National University
Cheong-ju, chung-buk, 361-763 Korea

Jungwoong Park, Sehyuk Ann and Namsoo Kim*
School of ECE, Chungbuk National University
Cheongju, chungbuk, 361-763 Korea
*nsk@chungbuk.ac.kr

***Abstract*—In this paper, a high performance current mode logic (CML) frequency divider is introduced in an integrated CMOS phase-locked loop (PLL). Inductive peaking structure and cascode circuit are applied in the CML frequency divider to obtain the broad-band and high frequency operation. In order to obtain a stable operation with low power, the resistor in the inductive peaking structure is replaced by the cascode circuit. DC bias voltage is applied in MOS gate as a current source in the divider. The proposed frequency divider is applied in the conventional PLL which is integrated with 0.18 µm CMOS process. Simulation test shows that the 2:1 divider is operated at the input frequency of 20 GHz with the power consumption of 15 mW.**

Keywords-Divider; Inductive peaking; Cascode; PLL; CMOS

I. INTRODUCTION

A frequency divider [1-4] is one of the important elements in a PLL system. It is used in many communication systems such as clock generation circuit and frequency synthesizers. The conventional analog PLL [5-6] is typically composed of phase detector, charge-pump, filter, VCO, and frequency divider. The generation of high frequency with low power depends mostly on the VCO and frequency divider.

Recently, several frequency dividers such as super-dynamic, injection-locked, and CML divider are introduced. Among these dividers, CML divider which is operated with master and slave latches exhibits a better performance than the other frequency synthesizer. In this work, the inductive peaking structure and the cascode circuit are introduced in the CML frequency divider. The cascode circuit works as the current source with high gain, while the inductor in the divider is supposed to provide the high operating frequency range. The application of cascode circuit can improve the power reduction in CMOS integrated circuit (IC) and reduce the on-off time-delay in the switching operation.

We designed the current-mode static frequency divider with operating frequency of 10 GHz in 0.18-µm CMOS process. The divider is applied in the conventional analog PLL and measurement is done in the CADENCE simulation.

II. CIRCUIT DESIGN OF DIVIDER

Typical CML frequency divider [4] as shown in Fig. 1 is composed with two level-sensitive CML master-slave latches. The operation of frequency divider in PLL is to reduce the output frequency of VCO to that of the reference clock so that phase detection can be carried out. Master-slave clocked flip-flop is commonly constructed in integrated circuit form. The state change of the master and slave takes place on the rising and the next falling edges of the clock pulse. The change occurs regardless of pulse width. Therefore, as long as the clock pulse width exceeds a certain minimum value, proper operation of the latch does not depend on pulse width and the error due to the rising and falling times can be protected. As shown in Fig. 1, the master-slave flip-flop operates as the read and latch circuits. The read circuit is the n-MOS differential pair and the latch circuit is the cross-coupled MOSFETs in the block. In digital integrated circuit, MOS differential pair is commonly applied as switch or comparator [7-8]. The divider exploits a common current source in the differential pair. The master-slave flip-flop is switched by the pair clock signals.

The application of inductive peaking technique [9-10] in the frequency divider can increase the operating range of frequency which can cover the VCO oscillation. In general, the inductive peaking extends a circuit bandwidth by inserting inductors, while it can delays the current flow. The inductor in series with the load resistor blocks the current flows at high frequencies, so that the pull-down current from the driver mostly flows into the load capacitor and the output can make a sharper transition.

Fig. 2 is the proposed CML frequency divider which has an inductive peaking structure. The cascode circuit is also used in the frequency divider in order to improve a current driving capability.

Application of inductive peaking [9-10] in CML master-slave latches is shown in Fig. 2 which is a conventional CML frequency divider with inductive peaking. Another application in the divider is the cascode circuit. The resistor in the inductive peaking circuit of the conventional CML frequency divider is replaced by the cascode circuit [11, 12] which is controlled by the DC bias gate voltage in MOSFET. In the integration circuit, a resistor with an accurate value is difficult to fabricate. The block of current mirror can be replaced as the current source instead of the resistor. The cascode circuit is the common-gate (CG) amplifier which usually applied to the common-source (CS) stage. It has the advantages of stable frequency response, variable resistance, and high gain. The switching peak current passing through

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the resistor can be significantly reduced by the proposed cascode circuit because the drain current in p-MOSFET is a small current under 10 mA.

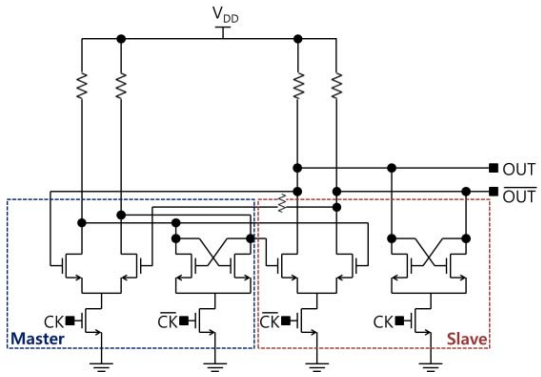


Figure. 1. Conventional CML frequency divider.

The cascode circuit in the integrated circuit (IC) can provide a small resistance across the transistor. Because the voltage drop across the transistor is small, the output swing is fully operational with small supply voltage. The time delay of the frequency divider can be significantly reduced by the cascode circuit.

Electrical study of the frequency dividers is done in the simplified circuit of the CS amplifier which constitutes in the frequency dividers. Fig. 3 shows the conventional and proposed structures, where the proposed one includes the inductor and cascade circuit.

The inductive peaking structure extends a circuit's bandwidth by inserting inductors that delay current flows. The inductor in series with the cascode circuit can cause the output voltage to have a sharp transition. The inductive peaking is known to degrade the time delay by increasing the bandwidth. The proposed structure has a cascode circuit instead of the resistor.

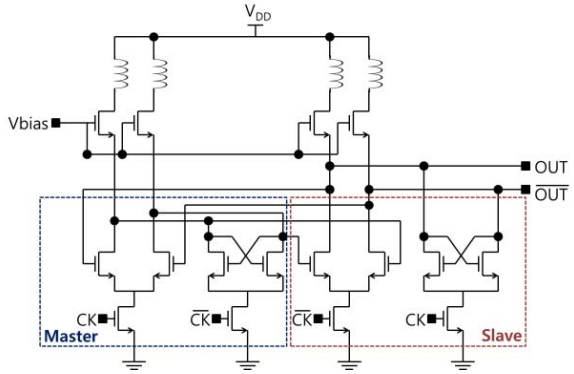


Figure. 2. Block diagram of the proposed CML frequency divider.

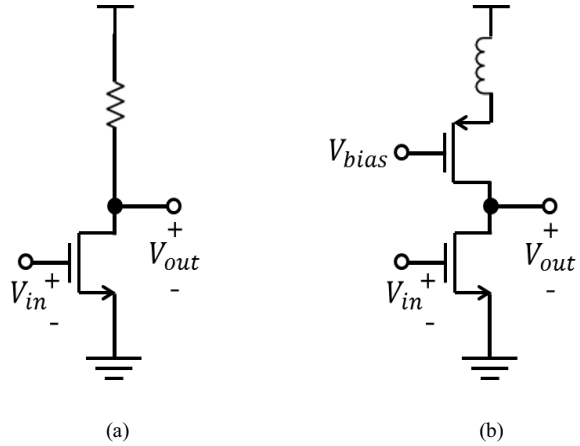


Figure. 3. Simplified circuit of the dividers (a) conventional (b) proposed.

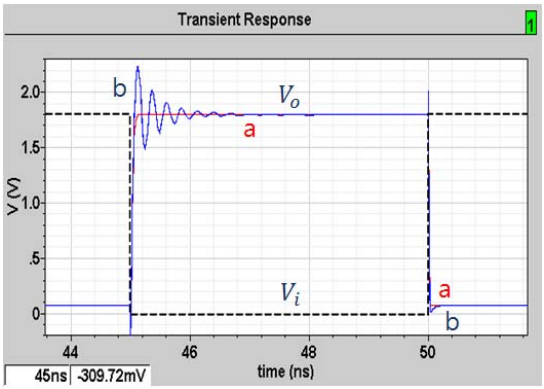


Figure. 4. Switching characteristic of the simplified circuit of the dividers (a) conventional (b) proposed.

The switching characteristic of the inductive peaking structure is shown in Fig. 4. The transient on-time is measured at 1 GHz frequency with variation of the inductance. The on-time-delay in the circuit with the inductance (a) is shown to be larger than that without inductor (c).

The cascode circuit can reduce the degradation of the time-delay in the inductive peaking structure. As mentioned, the cascode circuit is known to have the high equivalent gain which provides the variable resistance and improve the frequency response. The equivalent resistance depends on the small signal parameters of MOS transistor.

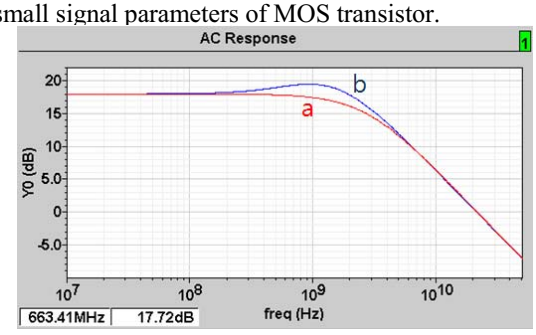


Figure. 5. Simulated Bode magnitude plot of the simplified circuit of the dividers (a) conventional (b) proposed

Fig. 5 is the simulated frequency response of the simplified circuit, where (a), (b), and (c) are mentioned before. The 3 dB bandwidth from the Bode magnitude plot is about 2 GHz in (c), while that in (a) extends to 3 GHz. The bandwidth in the circuit with inductance is increased, compared to that without inductance. With variation inductance in the inductive peaking structure, the bandwidth and time-delay are measured. Fig. 6 shows that the bandwidth and time-delay increase with increase of inductance. The expected results are obtained. The decay-constant during the switching depends on the parameters of the inductor and resistor. In series (parallel) connection of the two passive devices, the decay-constant increases (decreases) with increase of inductance.

Operating frequency and power consumption can be limited mostly by the transistor size. The interconnect resistor and parasitic capacitor should be minimized to obtain a high operating frequency with low power consumption. The current driving capability in the latch circuit is also an important parameter to decide the operating frequency and power consumption which are in the trade-off.

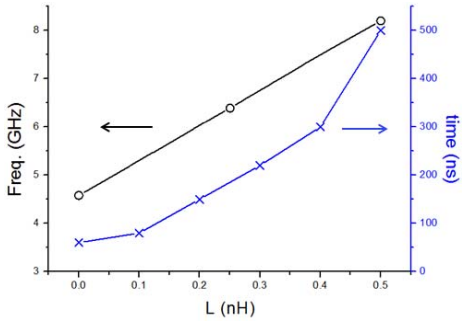


Figure. 6. The bandwidth and time-delay with change of inductance.

Fig. 7 is the block diagram of the odd and even dividers, where the control signal (Co) is included with the OR and AND gates. The even and odd dividers are the 2:1 and 3:1 static divider respectively. The 2:1 static divider in Fig. 7 is the proposed divider shown in Fig. 2. When the control signal is high (low), the even (odd) clock frequency can be obtained. Fig. 8 is the outputs of the even (/2) and odd (/3) signals at the frequency of 1GHz and the input of 1.8 V.

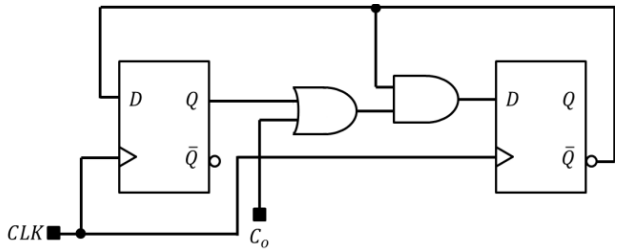


Figure. 7. Block diagram of the odd(/3) and even (/2) divider.

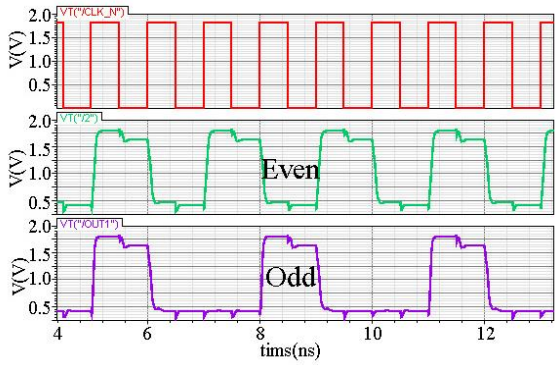


Figure. 8. Simulated result of the even and odd frequency divider.

III. RESULT

PLL is presented in Fig. 9 (a). It consists of a phase frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage controlled oscillator (VCO), and frequency divider. It has been designed in 0.18 µm CMOS process with 1.8 V supply. Fig. 9 (b) is the test circuit which has the frequency divider and phase frequency detector (PFD). The input in the frequency divider is supposed to be the output of VCO. The circuit of PFD is consisted of D flip-flops and AND gate. The role of PFD is to send the up or down signals to charge pump. Simulation work about PLL which includes the feedback frequency divider may provide a worse frequency characteristic, compared to the result from the test circuit of Fig. 9 (b).

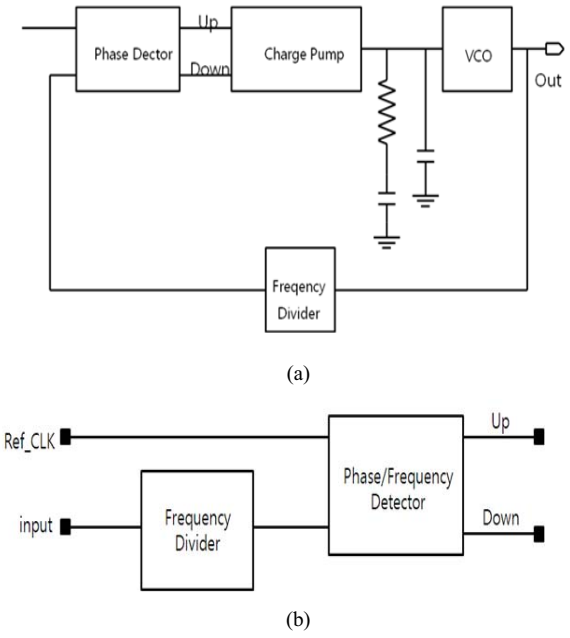


Figure. 9. (a) conventional PLL sutrcuture, (b) simplified circuit to test the frequency divider

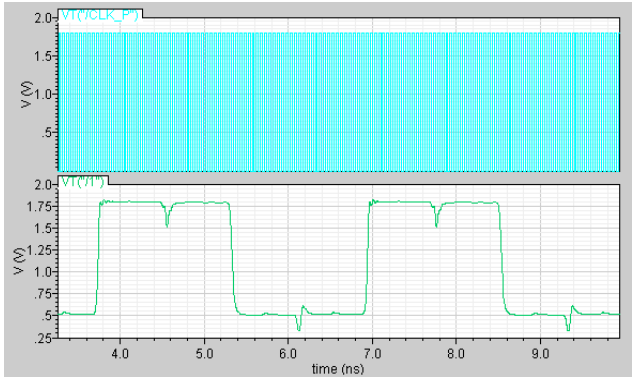
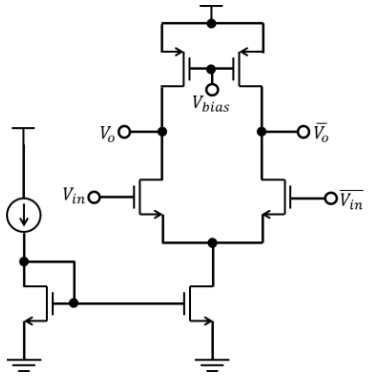
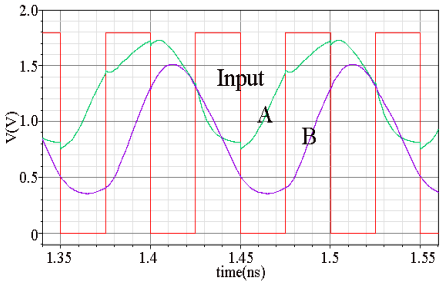


Figure. 10. Output waveform after six stages of 64:1 divider at the input of 16.6 GHz. Input sensitivity with variation of frequency.

Fig. 10 is the output waveform after six stages of even divider at the input frequency of 16.6 GHz. The simulation is done by the CADENCE Spectre. The 64:1 divider shows the proper operation of the proposed divider, on the other hand, with the conventional divider in Fig. 1, the same output waveform can't be obtained at the same input frequency of 16.6 GHz. This comes from the inductive peaking which provides a wider bandwidth in frequency response and results in a higher operating frequency.



(a)



(b)

Figure. 11. (a) Circuit of buffer in the proposed divider, (b) Output waveforms (A) without and (B) with buffer.

The output buffer in the frequency divider can provide a more stable output, although it cost a larger power consumption or die-area. Fig. 11(a) and (b) shows the circuit of buffer and output waveforms when the divider incorporates with and without buffer. Fig. 11(b) indicates that buffer provides a more stable wave form with large swing. It is obtained at the input of 20 GHz with the proposed 2:1 divider.

The input sensitivity of the divider is shown in Fig. 12. The maximum input power 2 dBm is obtained at 6GHz, while the required input power at 18 GHz is about -29 dBm.

The output spectrum of divider at the input frequency of 18.4 GHz is shown in Fig. 13, where (a) is the spectrum with the proposed divider which has the inductive peaking structure, while (b) is the spectrum with the conventional divider. In (a), the peak spectrum is obtained at the frequency of 9.2 GHz, which means that the 2:1 odd divider works properly at the input frequency of 18.4 GHz. The peak spectrum has the output power of – 9 dBm. On the other hand, Fig. 13 (b) shows the peak spectrum is obtained at 6.5 GHz. The peak spectrum should be obtained at 9.2 GHz which is the half value of the the input frequency 18.4 GHz. It indicates that the inductive peaking structure has a higher operating frequency because of the wider bandwidth.

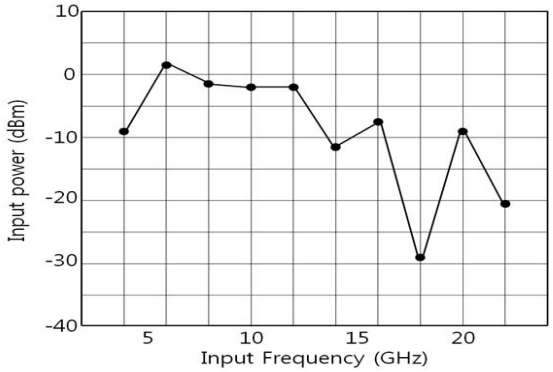
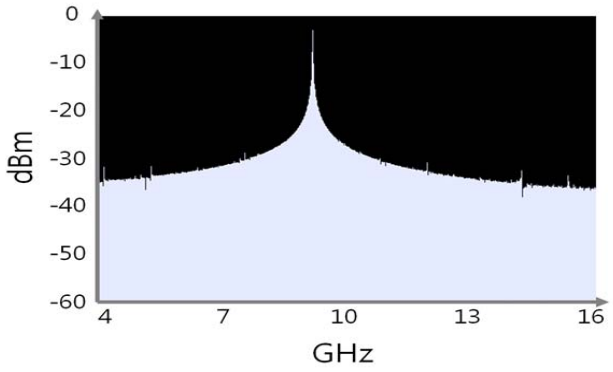
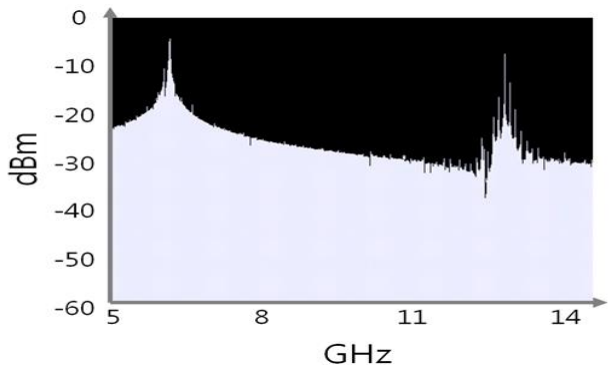


Figure. 12. Input sensitivity with variation of frequency



(a)



(b)

Figure. 13. Comparison of the output spectrum of divider from 18.4 GHz input frequency (a) proposed divider, (b) divider without inductive peaking.

IV. CONCLUSION

A In this paper, the inductive peaking with cascode circuit is proposed in CML frequency divider which operates with master-slave flip-flops. The cascode circuit is applied in the inductive peaking structure to replace the resistor. Simulation study in 0.18-µm CMOS process shows that the proposed divider shows a better performance in the output spectrum with input frequency of 18.4 GHz. In the study of switching characteristics and bandwidth with the simplified circuit, the inductive peaking structure provides a wider bandwidth, while the time delay becomes longer with increase of the inductance. The power consumption of the proposed divider at the input voltage of 1.8 V is about 6.9 mW.

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