LMSE-Based Voltage Regulation and Profile Optimization for Maximum Distributed Generation Penetration

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Abstract—There is general consensus among power systems researchers and engineers that integration of the ever-growing levels of distributed generation resources onto the conventional grid poses the most potent challenge to the operation of the next-generation grid. As a result, in order to accomodate high penetration, there is need for deployment of dynamic and active control technologies within equipment in the distribution layer. In this paper, an LMSE (Least Mean-Squared Error)-optimized voltage\((V_I)\)-voltage\((V_W)\) droop control scheme is proposed as the control algorithm for a back-to-back converter. The control function seeks to optimally regulate the secondary circuit voltage, internal dc-link voltage and feed-in current so as to obtain the objective of maximizing the distributed generation penetration levels for a given secondary circuit and its set of parameters. In order to achieve this, the converters and their controllers are modelled as a stage in cascade with a benchmark LV distribution circuit; and subsequently simulated in MATLAB. Simulation runs for three test cases are performed, and the optimality of the results for each test case are evaluated based on the profile voltage Mean-Squared Error (MSE) analysis. It can hence be deduced that in this paper, optimal droop control of a back-to-back converter can be leveraged so as to maximize DG penetration within the LV reticulation.

Keywords- Distributed power generation, Automatic voltage control, Back-to-Back Converters, Smart grids.

I. INTRODUCTION

Within the distribution system of the grand power delivery grid, there has been a rapid increase in the deployment and adoption of distributed generation sources like wind turbine generators, micro CHP units and solar PV systems. This is mainly attributed to favorable national and regional energy policies, increasing concern about the environmental effects of fossil fuels, security of energy supply, and most importantly, technological advances that have led to reduced costs. However, this has posed new grid challenges in some developed countries like Japan and Germany, whereby the penetration levels on some feeders have exceeded the system design limits [1]. This has necessitated active power curtailment [2] in order to prevent: i) overvoltage violation at the weakest nodes, and ii) thermal stress/overload or iii) costly grid reinforcement.

Several interconnection impact studies have identified voltage rise as a key limiting factor to the maximum penetration of DG resources that can be coupled to a feeder system [3]. This challenge is more pronounced in the generally passive distribution system of the conventional grid, whose performance greatly deteriorates amidst intermittent, inertia-less DG sources and their associated random power and voltage fluctuations. In [4], mathematical models for the maximum permissible DG penetration on a radial line are developed. In [5], a multi-objective programming approach to maximizing DG penetration is suggested. In [6], topology reconfiguration approaches, are proposed in order to maximize permissible DG penetration. A different approach based on optimal locating of DG units as a trade-off for investing in active network management schemes is introduced in [7]. Voltage-oriented approaches have also been severally suggested in various literature. For example, in [8], control mechanisms have been proposed to deal with the voltage constraint as means of increasing DG penetration capacity. At the MV level, active voltage control is mainly performed by on-load tap changing and reactive compensation along the feeder. Some studies [9] have proposed DG units with reactive power support coordinated with active power curtailment capabilities, and functioning as decentralized active controllers within a smart grid environment. Other studies [10] have evaluated the use of series controllers for voltage control; but all these have all been conducted at the MV level.

In the case of LV reticulation which is generally characterized by a low line reactance to resistance ratio, i.e. \(X/R\), and hence a high propensity for voltage rise amidst increasing DG active power, there is hardly any real-time component for active voltage control. A few studies have tried to address this issue in the LV network. In [11], a series reactor is...
introduced in the line so as to increase the $X/R$ ratio.

In [12], energy storage has been fronted as a solution for voltage support in LV grids with high penetration of PV units.

From the perspective of voltage profile characteristic improvement, some studies have been undertaken with regards to optimizing tap changer settings. For example, in [13], in order to maximize DG penetration in distribution systems, an advanced voltage regulation method for On-Load Tap Changers (OLTC) has been proposed.

However, this paper proposes a dual-purpose control scheme with the objectives of maximizing the penetration levels as well as improving the voltage profile. It is essentially an LV-based droop control scheme for a back-to-back converter architecture connected in cascade as a stage between the MV/LV transformer and the radial LV line. Back-to-back converters have been fairly well studied as power flow controllers in MV distribution networks [14-15]. In contrast to these studies, the control objective function of the back-to-back converter in this paper purposes to alter the upstream voltage for maximum penetration in either of the following modes, that is: 1) weakest node voltage, $V_{W}$-dependent mode or 2) feed-in current, $I_{FD}$-dependent mode. Unlike the weakest node voltage-dependent mode, the feed-in current dependent mode does not require any communication links because it depends on only local measurements at the converter terminals. Also, in order to quantify the performance improvement in the voltage profile characteristic, the mean-squared error (MSE) metric is introduced. The MSE analysis is evaluated for all three test cases and the most optimal control scheme in terms of voltage profile characteristic performance at different DG penetration levels is illustrated as one with the Least Mean-Squared Error (LMSE) plot.

Hence from both control schemes, an extra margin of active power can be coupled onto the feeder while in the case of the optimized control, the voltage profile is also improved such that the extreme node voltages are as close as possible to the nominal voltage, and the controller is as far away from its control limit.

This paper is organized as follows: Section II highlights the system overview. Section III describes the control strategy. In section IV, the simulation results performed on a European benchmark LV feeder [16] are presented. In this same section, MSE analysis of the control schemes is also explained. And the conclusions are presented in section V.

II. System Overview

The system architecture is as shown in the block diagram in Fig. 1 above, with the two proposed 3-phase converters of H-bridge topology connected back-to-back i.e. transformer-side converter and load-side facing converter. These converters are connected as an intermediate stage between the MV/LV transformer and the LV secondary circuit.

Downstream this secondary circuit / LV reticulation, there are consumer loads with DG sources whose capacity sizing is proportional to the respective coincident peak loads at the Points of Common Coupling (PCC).

III. Control Strategy

For each converter, there is an associated control subsystem. Both subsystems are based on PI controllers that operate on synchronous rotating d-q reference frame variables. These control subsystems output modulating reference signals, $V_{m\_ref}$, that the PWM generators use at their input in order to generate gate pulses to drive the converters as per the control logic.

A. Load-side Converter Control Subsystem

The load-side facing control subsystem’s objective is to regulate the upstream voltage, $V_{U}$ at the output of the load-side facing converter. This subsystem contains two controllers, i.e. a $V_{U}/V_{W}$ voltage droop controller and a PI controller. The output of the $V_{U}/V_{W}$ voltage droop controller is the set-point upstream voltage, $V_{U-S\_P}$ that

![System block diagram showing the distribution transformer, back-to-back converters, and the secondary circuit with consumer loads and DG units](image)

Figure 1. System block diagram showing the distribution transformer, back-to-back converters, and the secondary circuit with consumer loads and DG units
is used as the reference for the PI controller. In order to generate this set-point, i.e. $V_{U-SP}$, there are two control cases used:

- **CASE I**: In this case that evolves from our preliminary study [17], the weakest node voltage, $V_W$, that is usually at the tail-end of the radial line or branch is measured remotely via communication links, and applied to the droop controller with a characteristic similar to Fig. 2; which is also alternatively modelled in discrete-form by (1), (2) and (3).

\[
V_{U-SP,k+1} = \begin{cases} 
V_{U,k}^- & (V_{W,k} > V_{th}^+), \\
V_{U,k}^* & (V_{th}^- \leq V_{W,k} \leq V_{th}^+), \\
V_{U,k}^+ & (V_{W,k} < V_{th}^-). 
\end{cases} 
\tag{1}
\]

\[
V_{U,k}^* = V_{U,k-1} - m(V_{W,k} - V_{LC}) 
\tag{2}
\]

\[
V_{U,k}^{**} = \frac{V_{th}^+ + V_{th}^- + V_{U,k-1} - m(V_{W,k})}{2} 
\tag{3}
\]

where $V_{U-SP,k}, V_{U,k}$ denote the set-point upstream voltage and the weakest node voltage at the $k^{th}$ time-step respectively, $m$ is the droop factor and $V_{LC}$ is the pre-determined load-center voltage used in the normal control case in (2). $V_{U,k}^*$ is set-point for the normal control case whereas $V_{U,k}^{**}$ is the set-point from the equidistant extrema control case. The droop factor/slope, $m$ can be chosen depending on the desired sensitivity to change in weakest node voltage, $V_{W,k}$; however this comes with a trade-off against the resolution set point and stability margin.

It is important to note that unlike our earlier study [17] whereby the droop equation uses a memory-based voltage balancing value, in this paper, the droop equation for the normal case is based on the desired load-center voltage, $V_{LC}$. Hence, due to the memoryless nature of the load-center voltage setting that is used as a reference parameter in the droop equation, this greatly simplifies the implementation.

- **CASE II**: In this case, feed-in current, $I_{FD}$, that is locally measured at the converter terminals, forms the basis for the control. By substituting in (4) for this $I_{FD}$ and $V_U$, that’s also locally measured, the weakest node voltage, $V_W$ can be estimated. It is somewhat similar to the Line Drop Compensation (LDC) method for On-Load Tap Changers (OLTC), however unlike LDC, it does not explicitly use equivalent impedance and load-center voltage since these parameters are not static under DG-coupled feeders[13], but rather vary depending on the network operating states. Basing on the equidistant extrema control in (3), $V_{drop}/I_{FD}$ characteristics, for the benchmark secondary circuit used in this study, are pre-determined and plotted in Fig. 3. It can be seen that these characteristics are of the general form in (4).

\[
V_W = V_U + sI_{FD} 
\tag{4}
\]

whereby $s$ is the slope in Fig. 3, and its range varies for each secondary circuit depending on its topology, line impedance parameters, expected reliability or number of offline DG units at a time and the total capacity of the interconnected DG units. Basically, it varies from one LV reticulation circuit to another. Once $V_W$ is determined, it is henceforth applied in (2) or (3) in order to obtain a set-point $V_{U-SP}$ for the subsequent PI controller stage.

It is also important to highlight that while our earlier study [17] was exclusively based on remote measurements to establish the weakest node voltage $V_W$, in this paper, a control strategy based on local measurements is introduced as case II.

Using either remote voltage-based control (i.e. case I) or local current-based control (i.e. case II), two sub-cases of control could be leveraged for voltage profile improvement:

1) **Normal Control Sub-case**: This case is similar to the existent Automatic Voltage Regulator algorithms, whereby the voltage, $V_{LC}$ is regulated and kept constant at a pre-determined load-center along the line. This is represented in (2).

2) **Equidistant extrema balancing Sub-case**: This algorithm is based on making the two extrema of the node voltages equidistant from the overvoltage limit, $V_{th}$.
and undervoltage limit, $V_{th}^-$ respectively; or balanced about the nominal voltage, $V_{nom}$. The objective is to ensure that the service voltages at the different nodes are as close as possible to the nominal voltage, and that the controller operating point is as far away as possible from the control limit. In other words, it does not focus on a particular load-center’s voltage regulation like conventional LDC algorithms, but rather on the two extreme nodes’ voltage management. This is represented in (3) above, or alternatively, as a function of $V_{nom}$ in (5) and (6).

$$V_{TOL} = V_{th}^+ - V_{th}^-$$

$$\Delta V_{k-1} = \frac{V_{W,k-1} - V_{U,k-1}}{2}$$

$$V_{U,k} = V_{nom} - \Delta V_{k-1}$$

$$V_{U-SP,k} = \left\{ \begin{array}{ll}
V_{th}^+ & \text{if } (\Delta V_{k-1} < -V_{TOL}), \\
V_{th}^- & \text{if } (-V_{TOL} \leq \Delta V_{k-1} \leq V_{TOL}), \\
V_{th}^- & \text{if } (\Delta V_{k-1} > V_{TOL}).
\end{array} \right. \quad (6)$$

where $V_{nom}$ is the nominal voltage around which the extremas are balanced, and the rest of the parameters retain the same definition as in (1), (2) and (3).

Basically, from the aforementioned control methods, the output is the desired set-point, $V_{U-SP}$ for the subsequent PI controller. From the PI-controllers, modulating signals, $V_{m-ref}$ are generated and fed to the PWM generator so as to ensure that the load-side facing converter voltage tracks the set-point upstream voltage. This PI controller’s parameters are derived from an approximate open-loop model without second-order terms in (7), and further refined by Ziegler Nichols tuning method in order to obtain the appropriate respective proportional and integral gains.

$$V_{m-ref}^d = \frac{V_{dc}}{2} (V_{ad} + \frac{L_f}{R_L} \frac{dV_{ad}}{dt} - w \frac{L_f}{R_L} V_{aq})$$

$$V_{m-ref}^q = \frac{V_{dc}}{2} (V_{aq} + \frac{L_f}{R_L} \frac{dV_{aq}}{dt} + w \frac{L_f}{R_L} V_{ad}) \quad (7)$$

This model(7) is based on cross-coupled synchronous $dq$ reference frame variables, where $V_{dc}$ is the dc-link voltage, $V_{m-ref}^d$, $V_{m-ref}^q$, $V_{ad}$, $V_{aq}$, are the $d$-axis and $q$-axis components of the respective variables as described in the nomenclature, $w$ is the nominal angular frequency, $L_f$ is the filter inductance, and $R_L$ is the secondary circuit’s equivalent output impedance respectively.

A closed-loop PI control algorithm based on the model in (7) can be defined in its discrete form as in (8) and (9).

$$V_{m-ref}^d = K_p \Delta e^d_q + K_i e^d_q \Delta t + (Y_{PI,k-1})^d_q - w \frac{L_f}{R_L} V_{ud}$$

$$\Delta e^d_q = e^d_{q,k} - e^d_{q,k-1}$$

$$e^d_{q,k} = V_{ud-S_P,k} - V_{ud} \quad (9)$$

$$\Delta t = t_k - t_{k-1} = T_s$$

whereby superscripts or subscripts of $d$ and $q$ correspond to the $d$-axis and $q$-axis components of the respective variables, subscripts $k$ and $(k-1)$ represent the $k^{th}$ and $(k-1)^{th}$ timestep respectively, $\Delta t$ is the discrete timestep, $K_p$ is the proportional gain, $K_i$ is the integral gain, $V_{ud-S_P,k}$ denotes the set-point upstream voltage from (1) and $Y_{PI,k-1}$ is the previous time step’s PI controller output (in dimensions of per unit voltage).

B. Transformer-side Converter Control Subsystem

The transformer-side controller’s overall objective is to regulate the feed-in current as well as the dc-link voltage. Essentially, it has an outer dc-link voltage loop, modelled by (10) in order to determine the set-point feed-in current for the inner current loop, that is necessary for tracking the reference dc voltage at the dc link.

$$Y_{PI,k} = Y_{PI,k-1} + K_p \Delta e + K_i e \Delta t$$

$$I_{XFMR-SP,k}^d = \frac{I_{FDMUXFMR}^d + I_{FDMUXFMR}^d V_{uq}^{XFMR} - Y_{PI,k}}{V_{XFMR}^{dc}}$$

$$I_{XFMR-SP,k}^q = \frac{I_{FDMUXFMR}^q - I_{FDMUXFMR}^q V_{uq}^{XFMR}}{V_{XFMR}^{dc}} \quad (10)$$

whereby $V_{DC-REF}$ denotes the reference dc-link voltage, $I_{XFMR-SP,k}^d$ is the desired set-point transformer side current that serves as the reference for the subsequent PI controller in (11), $Y_{PI,k}$ is the $k^{th}$ time-step’s PI controller output (in dimensions of power) and the rest of the terms denote the same meaning as previously declared.

The inner PI-controlled current loop is of the same general format as in (8) however it contains a feedforward term, $E_{d}^q$ as shown in (11). It is also tuned by the Ziegler Nichols method so as to track the set-point current signal, $I_{XFMR-SP,k}^d$ from the preceding dc-loop stage by generating appropriate modulating signals, $V_{m-ref}$ for the PWM generator driving the transformer-side converter.

$$V_{m-ref}^d = K_p \Delta e^d_q + K_i e^d_q \Delta t + (Y_{PI,k-1})^d_q - C_d^q + E_{d}^q \quad (11)$$

$$e^d_{q,k} = I_{XFMR-SP,k}^d - I_{XFMR-SP,k}^d$$

$$C_d^q = w \frac{L_f}{R_L} V_{ud} \quad (12)$$
whereby $C_d^+$ is the cross-coupling term, $E_q^d$ is the measured voltage at the transformer terminals, $I_{XPM}^d_{SP,k}$ denotes the set-point transformer-side current from (10) and the rest of the terms retain the same meaning as in (8). A virtual output resistance, $r_v$ [18] is used in order to improve system stability by quickly damping any system transients.

IV. RESULTS

The effectiveness of the aforementioned control strategies on the intermediate back-to-back converter stage was validated by simulation in the MATLAB/Simulink/ SimPowerSystems platform and also by a forward-backward load flow program that was run on the benchmark radial feeder [16]. The DG units were connected at unity power factor. The voltage tolerances are ±10% as per the EN 50610 European standard. A worst case scenario is assumed whereby light loading operating states coincide with peak DG output. In this paper, the DG penetration level is defined as the ratio of the DG capacity to the secondary circuit’s coincident peak load.

Three test cases are evaluated, i.e.:

- **TEST CASE A**: Without the proposed intermediate converter stage, load flow analysis is performed on a baseline LV feeder [16] for different DG penetrations ranging from 0% to 450%. The weakest node’s voltage profile at different penetration levels, for this test case is shown in Fig. 4 (i.e. red line), with a maximum penetration of 210% at the overvoltage limit. In Fig. 5 (i.e. first subplot from the top), the steady-state nodal voltages, $V_{PCC}(p.u)$ at the different PCCs are plotted, based on time-series data extracted from the Matlab model simulation of this baseline test case. The penetration, $DG_p(\%)$, is varied in step units of 50% every 1s, from 100% to 450%.

- **TEST CASE B**: With the proposed intermediate converter stage but using remotely measured weakest voltage, $V_W$-based control, the maximum permissible penetration is increased by 140% from 210% (cf. red plot, Fig. 4) to 350% (cf. green and black plots, Fig. 4) before overvoltage violation, i.e $\Delta DG_p = 140\%$. This can be attributed to the active voltage control of the back-to-back converters in response to the DG output levels.

- **TEST CASE C**: This test case is similar to test case B, however the droop controller action is based on the locally measured feed-in current, $I_{FD}$, in order to estimate the weakest node voltage, $V_W$. In this test case, similar results to those of $V_W$-based control in test case B are obtained, as shown in Fig. 5 (i.e. second plot from the top). As in test case A, the penetration, $DG_p(\%)$, is varied in step units of 50% every 1s, from 100% to 450%. And it can be observed that the weakest node also breaches the overvoltage threshold at $DG_p = 350\%$; just as it was for the $V_W$-based control (black and green lines, Fig. 4). However, unlike $V_W$-based control, the added benefit to this test case is that no communication links are required, i.e. only local measurement of variables.

It is important to note that the upper three sub-plots of Fig. 5 are color-coded according to the particular nodes/points of common coupling to the LV circuit i.e. the blue plots represent PCC#1, that is electrically closest to the back-to-back converter; while the plots in magenta represent PCC#5 which happens to be the weakest node in our set-up and also the furthest electrically from the back-to-back converter in a radial network configuration. The other colored plots represent PCCs in between these two extreme nodes.

With regards to voltage profile improvement, Fig. 6 indicates a comparative analysis of the profile-improvement effectiveness of the control strategies. For illustration of the results, an arbitrarily chosen DG penetration level of 250% , and load-center voltage $V_{LC}(p.u)$ of 1.08 are considered. Without the back-to-back converter based control (cf. blue line, Fig. 6), nodes 3, 4 and 5 experience overvoltage. On the contrary, for both control cases (i.e. green and red plots, Fig. 6), all nodes are within the safe voltage operating range. However, for the normal load-centered control, i.e. without equidistant extrema balancing method (green line, Fig. 6), it is seen that the profile is not balanced, and as such the weakest node is closer to the overvoltage limit. In contrast to this, the control strategy with equidistant extrema balancing (red solid line, Fig. 6), the voltage profile is evenly balanced about the nominal voltage and all nodes are safely within the safe operating voltage range.

In Fig. 7, weakest node voltages, $V_W(p.u)$, of the 3 subcases i.e. without control, with normal control and with equidistant extrema balancing control, are directly compared on the same axes as functions of increasing $DG_p$ levels. It can be seen that for the baseline system without the proposed converter, the weakest node voltage (black plot, Fig. 7) breaches the designated upper limit, $V_{th}^+$ for DG penetration levels just above 200%. However, in the case...
of a feeder with the proposed converter stage, for either of the control strategies, the weakest node voltages, $V_W$ (blue and green lines, Fig. 7) breach the overvoltage threshold at DG penetration, $DG_P$ of 350% and above. However, in normal control (blue plot, Fig. 7), the weakest node voltage is maintained at the load-center voltage setting, which is often close to the limit depending on the load center point on the secondary circuit. Thus, it is evident that the proposed converter can also be used to maximize DG penetration without overvoltage stress as well as improve the voltage profile.

Fig. 5 also contains two additional subplots: at the bottom is a subplot of extracts of 4 cycles of the feed-in current $I_{FD}$ corresponding to each DG penetration step. And second from bottom is the droop controller output i.e. the setpoint upstream voltage $V_{U - SP}$ that is the subsequent PI controller’s reference, that regulates the secondary circuit voltage as a function of $DG_P$.

Table I is a summary of comparative results for the weakest nodes steady-state voltages for the three control strategies at the different stepped DG penetration levels. The results in Table I reflect the illustrations in Fig. 5 (only of the weakest node plots - in magenta).

### Table I

<table>
<thead>
<tr>
<th>$DG_P$ (%)</th>
<th>$V_W$ (pu) without Control</th>
<th>$V_W$ (pu) with Normal Control</th>
<th>$V_W$ (pu) with equidistant extrema Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>1.0255</td>
<td>1.0832</td>
<td>1.0124</td>
</tr>
<tr>
<td>150</td>
<td>1.0617</td>
<td>1.0804</td>
<td>1.0306</td>
</tr>
<tr>
<td>200</td>
<td>1.0956</td>
<td>1.0802</td>
<td>1.0485</td>
</tr>
<tr>
<td>250</td>
<td>1.1277</td>
<td>1.0824</td>
<td>1.0670</td>
</tr>
<tr>
<td>300</td>
<td>1.1582</td>
<td>1.0867</td>
<td>1.0843</td>
</tr>
<tr>
<td>350</td>
<td>1.1873</td>
<td>1.1051</td>
<td>1.1064</td>
</tr>
<tr>
<td>400</td>
<td>1.2151</td>
<td>1.1338</td>
<td>1.1273</td>
</tr>
<tr>
<td>450</td>
<td>1.2419</td>
<td>1.1615</td>
<td>1.1547</td>
</tr>
</tbody>
</table>

Heretofore, profile improvement of the equidistant extrema control strategy has been evaluated at only an arbitrarily-chosen DG penetration level of 250%. In this paper, the performance improvement of the profile characteristic is further quantified by the MSE (Mean-Squared Error) metric as a function of varying DG penetration levels in step units of 10%, where by MSE is defined in (13).
whereby $N$ denotes the number of nodes or Points of Common Coupling of the DG sources onto the LV circuit, $\varepsilon_i$ is the voltage deviation from the nominal value at a given node, $i$, $V_{PCC}$ is the nodal voltage at the PCCs, and $V_{\text{nom}}$ is the nominal voltage.

A quantitative comparative analysis based on the MSE equation in (13) is performed for each of the three control cases i.e. the baseline case without the back-to-back converters, the normal control case based on load-center voltage, (i.e. $V_{LC}$-control logic), and the equidistant extrema control case. The best performing profile characteristic is that with the least MSE (LMSE) at the respective penetration levels; implying that all nodal voltages ($V_{PCC}$) are as close as possible to the nominal voltage in comparison to the other control cases.

From Fig. 8, it is evident that for all DG penetration levels, the equidistant extrema control strategy (i.e. the green plot with diamond linespoints) has the least mean-squared error in profile voltage as compared to the other control cases; hence representing the most optimal profile characteristic performance. The normal control case based on load-center voltage at low and moderate penetration levels which reduces to comparable levels as those of the optimal case at high DG levels. On the contrary, the baseline case, with neither a control scheme nor back-to-back converters (i.e. the black line with star linespoints), exhibits comparable profile voltage performance in comparison with the optimal case at low penetration levels; however its MSE value increases inordinately as DG penetration increases.

Hence, it can be deduced that the equidistant extrema control scheme not only results in increased DG penetration, but it also offers the most optimal profile characteristic for all DG penetration levels.

V. Conclusion

In this paper, the concept of a back-to-back converter as a voltage control intermediate stage between the MV/LV transformer and secondary circuit with DG sources has been introduced clearly. The converter’s controller logic has been explored. Both remote weakest node voltage-based control and locally measured feed-in current-based control have been discussed. Based on the system validation simulation results, it is deduced that for this benchmark set-up, permissible DG penetration can be increased by 140%, from 210% in a baseline feeder without this converter to 350% in a feeder with the proposed converter, without overvoltage violation.

In addition, a voltage profile improvement control strategy using the equidistant extrema algorithm has been discussed and compared to the normal control. Results have shown that the voltage profile can also be improved such that even the weakest nodes are as close as possible to the nominal voltage at all $DG_P$ levels, hence keeping the controller as far away as possible from its control limit, and increasing the voltage excursion margin.

Regarding future works, analysis of the performance of this proposed concept during grid disturbances is proposed. For better controller performance, advanced controllers like genetic optimal fuzzy controllers or adaptive neuro-fuzzy controllers could be used in these future works.

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**APPENDIX**

**NOMENCLATURE**

- $V_{th}^+$: Overvoltage threshold.
- $V_{th}^-$: Undervoltage threshold.
- $V_{m_ref}$: Reference modulating signal.
- $V_{X_{FMR}}$: Transformer-side converter’s voltage.
- $I_{X_{FMR}}$: Transformer-side converter’s current.
- $V_W$: Weakest node voltage.
- $V_U$: Secondary circuit upstream voltage.
- $I_{FD}$: Upstream feed-in current.
- $V_{LC}$: Load center voltage.
- $V_{PCC}$: Nodal Voltage at Point of Common Coupling.
- $DG_P$: Distributed Generation Penetration level.