Optimization Design of Weighted Built-In Self-Test based on Multi-Objective Genetic Algorithm

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***Abstract* — With a thorough investigation on design methods of Built-In Self-Test (BIST) applied for super large-scale integrated circuit, a novel method is proposed. In this method, the 1D hybrid cellular automata is taken as the core structure, based on which the entire BIST generator can be constructed. The rule set corresponding to cellular automata is optimized through genetic algorithms until the stop criterion is satisfied. One rule is selected from the optimum rule set, described by Verilog language and applied to cellular automa. After finishing these three steps, the whole BIST generator is burnt into FPGA to carry out the test. The experiments, which are carried out using ISCAS'85 as platform, demonstrate that the length of test sequence is prominently optimized on the condition that a high malfunction coverage ratio was ensured.**

Keywords - Cellular Automata, BIST Generation, Multi-objective Genetic Algorithms, Verilog

I. INTRODUCTION

In BIST applied to super large-scale integrated circuit, the test generator is very important. A clever design requires that many kinds of underlying circuit malfunctions can be stimulated with only a small set of test vectors sent to under-test circuit. During past years, many BISTs have been designed.

The core structure of BIST generator is finite-state machine (FSM). Linear shift register (LSR) and cellular automata (CA) are usually adopted as FSM. CA was first adopted by Wlofram in 1986 when designing a high-quality pseudo generator. Because CA has characteristics of simple structure, being in-order and local, it is more convenient for it to be applied to hardware compared with other model, for example linear shift register. The design of CA is quite flexible. In [3], a single weighted set is obtained through minimization or maximization based optimization. Although simple, this CA can not cover all the test specifications. In[4], the CA adopted has high efficiency, but the corresponding structure is very complicated. In[6], although a high ratio of test coverage can be obtained, too much hardware cost becomes a by-product caused by introducing linear shift register into CA. Therefore, in this paper, the multi-objective genetic algorithms are used to obtain an optimum combination set of test sequence length, power cost and mal-function coverage, based on which the suitable CA can be constructed[10].

Multi-objective genetic algorithm (GA) is a general technique that can be used to obtain the global optima. Because GA is highly parallel and multiple optimization results can be generated, compared with the traditional techniques, it is especially suitable for solving complicated problems. The procedure of GA can be divided into two steps. First, an objective function, taking interested physical description as variables, is obtained by transforming problem model mathematically. Second, optimum results can be obtained using random searching tactics[1-2].

II. MULTIPLE OBJECTIVES OPTIMAL MODEL

Being different from former linear shift register or hybrid CA-LSR model, the BIST generator proposed in this paper is completely based on CA model. At the same time, rule set corresponding to this CA is obtained through multi-objective optimization procedure and is optimum. Therefore, in this section, the principle of CA used in BIST will be explained, as given by Fig.1 [6].

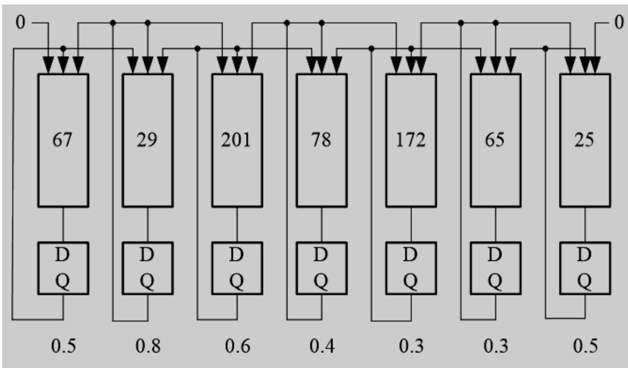

Figure 1. The CA Has 7 Cells

As Fig.1 tells, assuming that CA has 7 cells and the rule corresponding to each cell is numbered as 67, 29, 201, 78, 172, 65, 25 from left to right. According to characteristic of CA, different rule will generate bit output having different probability. In Fig.1, for each cell, the probability of outputting logical value '1' is 0.5, 0.8, 0.6, 0.4, 0.3, 0.3, 0.5, from left to right respectively. By changing one cell's rule, its probability of outputting '1' changes as well and thus the mal-function coverage probability will become different[5,7].

Applying rather short test vector to reach the relatively high fault coverage is conflicting. The mathematic operation is applied to drive the logic "1" to have deflection probability, which reduced the test length obviously on the

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premise of not decreasing the fault coverage. Its specific model is as follows:

$$\begin{cases} f_i(x) = \left| x_{atc} - x_{des} \right| \\ \sum_{i-1}^{n} f_i(x) \leq \Delta P_{sat} \end{cases}$$

The fi(x) refers to the test vector length; xact refers to any CA with the probability of "1"; xdes is expected probability; △Psat is allowable error. The specific process: set the CA rule set firstly, simulate the probability xact of "1" of every CA to minus its expected probability xdes to let the practical weight get closer to the expected value. The error sum of xact and xdes is ≤ △Psat. Then the weighted CA can be obtained. Optimizing the weighed CA can reduce the length of test vector.

By adopting multi-objective genetic algorithms, the optimum rule set can be obtained after finishing the procedures of evolution, selection, crossing and mutation until the stop criterion is satisfied. During the evolutionary process, by using equation $f_i(x) = \left| x_{atc} - x_{des} \right|$ as the objective function, the cell rule will gradually approach the optimum result and at the mean time the length test sequence generated by the optimum CA is small enough. Besides that, any two test sequence in each evolutionary generation should have weak correlations as much as possible and this ensures that the test set generated by CA in each generation will have higher mal-function coverage probability[9].

Any result in the group of optimum rule sets could be applied to CA, because Pareto sorting technique is used in multi-objective genetic algorithm. Please note that, initial GA parameters have severe influences on the final optimization results and thus the corresponding result of circuit testing might have a big difference.

Obviously, the CA structure obtained in this way is quite simple and no additional hardware is needed. Compared with LFSR, the weighted logical circuit can be removed. At the same time, the cross-correlation of test sequences is much smaller compared with LFSR, which is more convenient for CA to be used in super large-scale integrated circuit test.

III. Configuration of BIST

The intrinsic characteristic of BIST generator based on multi-objective genetic algoritchm lies in two aspects: first, the cell rules are optimized through GA; second, one optimum rule set is applied to CA, based on which the pseudo generator can be constructed[8].

The GA algorithm used in this paper is given in Fig.2 and the stop criterion is defined as the difference between actual and expected probability.

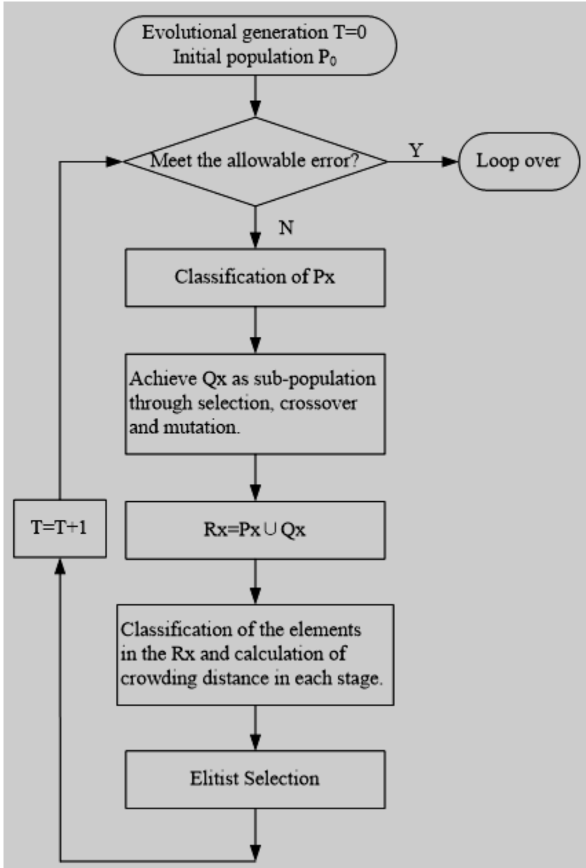

Figure 2. Multi-objective Genetic Algorithms Flowchart

The hardware configuration of BIST generator used here is given by Fig.3. In Fig.3, '1,2,..n' denotes the index of each CA and 'n' is the total number.

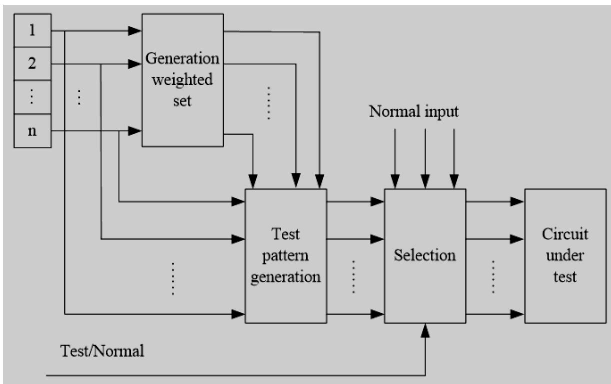

Figure 3. Structure Diagram of Test Pattern Generation

The rule set is generated through multi-objective GA and the probability corresponding to all the output bit stream approaches the ideal value. After generating one initial test sequence, the subsequent test sequence can be generated through weighted summarization. When the multi-pass circuit simulates the 'test ' function, the test sequences will been input into the tested circuit. The CA is implemented through Verilog and partial code is given below.

```
ca_next_state[2]
=(ca_now_state[1]&(~ca_now_state[2])&ca_now_state[3])|((~ca_now_state[1])&ca_now_state[2]&ca_now_state[3])|(~ca_now_state[1]&ca_now_state[2]&(~ca_now_state[3]));
//Rule 44
ca_next_state[29]=((~ca_now_state[29])&(~ca_now_state[30]))|((~ca_now_state[28])&(~ca_now_state[30]))|((~ca_now_state[28])&(~ca_now_state[29])&ca_now_state[30]);
//Rule 23
ca_next_state[30]=((~ca_now_state[29])&(~ca_now_state[30])&(~ca_now_state[31]))|((~ca_now_state[29])&ca_now_state[30]&ca_now_state[31]); //Rule 9
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IV. Experimental Results

The cross and mutation probability are listed in Table I.

TABLE I. SELECTED CROSS AND MUTATION PROBABILITY

The circuit to be tested	Crossover probability	Mutation probability
C432	0.85	0.01
C6288	0.85	0.01
C1908	0.844	0.01
C1355	0.845	0.01

TABLE II. CA RULE-SET

Circuit	Primitive polynomial	Seed
C432	36：25：0	f101bb288
C1355	41：3：0	aaaaaaaaaa1
C1908	33：13：0	44bd2a4b0
C6288	32：28：27：1：0	aaaaaaaa

The parameters of linear shift register are listed in Table III.

TABLE III. PARAMETERS OF LINEAR SHIFT REGISTER

Circuit	Port	Rule set
C432	36	189 210 131 141 30 210 46 44 174 230 112 253 7 241 138 128 137 10 63 72 87 17 233 227 213 26 73 18 70 251 103 102 55 13 134 212
C1355	41	196 108 156 74 241 48 148 165 145 194 93 108 129 184 48 222 216 12 177 58 4 62 76 84 252 126 88 176 74 55 247 172 127 129 229 82 183 96 90 10 169
C1908	33	32 157 89 102 169 41 18 25 82 103 150 207 87 109 19 143 26 153 155 37 145 138 125 93 164 79 193 242 138 113 37 86 78
C6288	32	156 70 44 251 14 87 191 164 241 216 118 41 143 95 71 9 88 26 102 53 171 143 114 58 37 143 208 33 18 23 9 65

In the experiment, the CA structure and testing stimulating files are realized using Verilog language in PC and modelsim is used to simulate. Taking C6288 circuit as an example, the simulating results are given by Fig.4.

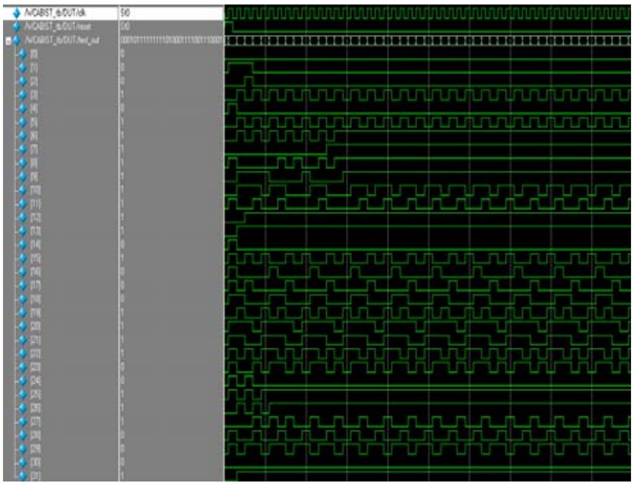

Figure 4.Simulation Waveform

In Fig.4, 'clk' denotes the clock signal, 'reset' is the reset signal, 'test_out' represents test sequence signal generated by CA. Totally 32 test sequences are generated. In the first cycle, reset signal is set to a high level. Then, the initial parameters are sent to the input of CA. After that, from the second cycle, the reset signal is set to a low level and CA starts generating test sequences.

The test sequences generated are applied to ISCAS'85 circuit and the experimental results are shown in Fig.5.

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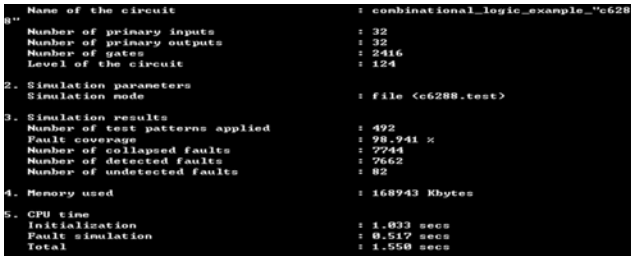

Figure 5. Results of Test Sequences Generated are Applied to ISCAS'85 Circuit

After finishing the testing on C432, C1355 and C1908, the results are listed in Table IV, which can be compared with the results generated through pseudo sequence generator.

TABLE IV. TEST DATA COMPARISO

Circuit	Primitive LFSR used for the generation of pseudo-random sequence		Test sequence generated by BIST	
	Length	Fault coverage(%)	Length	Fault coverage(%)
C432	2000	93.75	410	94.466
C1355	4000	94.50	642	96.633
C1908	2000	94.99	770	92.869
C6288	2000	99.34	492	98.941

V. CONCLUSION

According to Table.4, the introduction of multi-objective GA to the construction of CA is successful. On the condition that the mal-function coverage was not sacrificed, the length of test sequence can be effectively reduced. At the same time, the reduction of test sequence length also makes the power cost used for testing decrease as well.

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