An Implementation Method for Low Frequency Digital Oscillator

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***Abstract* — A low frequency digital oscillator structure is proposed which employed two multiple output digital oscillators with error feedback network. The performance is improved and roundoff error is analyzed. The oscillator has the extremely low frequency andlarge number sample frequency. The application of proposed oscillator for a telecommunication system, such as complex baseband FSK modulator, is discussed and simulated using MATLAB program. The simulation results show that the designed extremely low frequency oscillator is appropriate for applications, especially in situations that demand the use of very low frequencies.**

Keywords - Low frequency digital oscillator; Low frequency digital oscillator; FSK modulator

I. INTRODUCTION

The digital sinusoidal and cosinoidal signals are the most basic signals which have a widespread of applications in DSP areas, such as music synthesizing, signal modulation, DTMF signal generation in Telecommunication, and control system. Digital oscillator is the most basic technique to generate the digital sinusoidal and cosinoidal signals, which already developed a plenty of technologies with the development of some new DSP algorithms and hardware realization techniques [1].

Conventionally there are four methods to generate sine and cosine signals. The first one is lookup table which stores the amplitude samples in a ROM (read-only memory) then read the samples from ROM at suitable time intervals [1]. The second one is based on the CORDIC (Coordinate Rotational Computer) algorithm which is an iterative digital algorithm, it allows rapid rotation of coordinates in digital plane and can be used for the calculation of trigonometric function [2]. The third method is approximation of the sine or cosine function by a polynomial [1]. The last method is employed a second order recursive digital filter which is using in our work. It is very remarkable efficient when compared the last technique with others. Many of research papers for the oscillator have employed the second order recursive digital filter. The first paper regarding this filter on oscillator was studied in the work of [4,5]. For fixed point processing digital oscillator, the multiplier coefficients and the outputs of arithmetic operations must be quantized to fit in the allocated word length [3]. In the work of [3], an error feedback method was used to reduce the round-off noise, and makes the second order recursive digital filter efficiency to implement oscillator. An extremely low frequency digital oscillator in [6,7] employed two multiple-output digital oscillators to synthesis the output sinusoidal which using the trigonometric identities. The paper in [8,9] proposed a digital oscillator used the sign switching technique to reduce the coefficient of multiplier when fixed point implementation it. In the paper of [10,11], a one more rounding operation for coefficient multiplier quantization after sign switching is used to reduce round-off error efficiency. This paper proposed the digital oscillator base on changes the multiple-output direct form oscillator structure of [6] instead of [10], and utilize a second order error feedback network for multiple-output digital oscillator, then gives up the LBF what [6] be used.

II. SHORT REVIEW ALGOTITHM DEVELOPMENT OF OSCILLATOR

In the digital domain, the digital sinusoids obey a second-order difference equation using the trigonometric identities:

$$\sin(\alpha+\beta)=\sin\alpha\cos\beta+\cos\alpha\sin\beta \quad (1)$$

This can easily be shown below,

$$\sin(\Omega(t-2T))+\sin(\Omega t)-2\cos(\Omega T)\sin\Omega(t-T)=0 \quad (2)$$

From Eq. (2), we can get the following digital form equation.

$$y(n)-2\cos(\Omega T)y(n-1)+y(n-2)=0 \quad (3)$$

In order to design a digital oscillator, we can assign the intended frequency value at $2\cos(\theta)$ with $\theta = 2\pi f/F$. Note, f, is the desired frequency in cycles per second, while F is the clock frequency. The number of samples in complete cycle of the sine or cosine waveform is given by $N=2\pi/\theta$. The largest sample number is given when θ has a minimum value $\theta_{min.}$

A. Oscillator to Generate Sine and Cosine Wave

In digital domain, because sinusoids obey the Eq. (3), next we use the DSP tool to exploit the Eq.(3) how to output sinusoidal. By using Z transform, Eq.(3) is given as,

$$Y(z)=[(2\cos(\theta)-z^{-1})y(-1)-y(-2)]/(1-2\cos(\theta)z^{-1}+z^{-2}) \quad (4)$$

If we set the initial condition $y(-1)=-A\sin(\theta)$, $y(-2)=A\sin(2\theta)$ and substituting them into (4), then taking the inverse z transform, we will get sine wave, $y(n) = A\sin(n\theta)$. The implementation structures is showing in Fig.1.

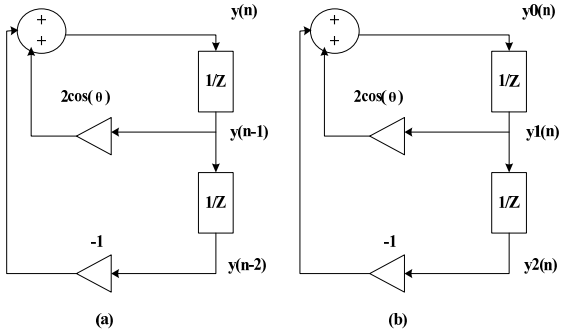

Fig. 1 (a) The Structure of sine oscillator, (b) The structure of cosine oscillator

From Fig.1 we can get $y_1(n)=y(n-1)$, By taking Z transform above $Y1(Z)=Z^{-1}Y1(Z)+y(-1)$,**Error! Reference source not found.** then arrange it getting ,

$$Y_1(z)=[y(-1)-z^{-1}y(-2)]/(1-2\cos(\theta))z^{-1}+z^{-2}) \quad (5)$$

Set initial conditions $y(-1)=1$, $y(-2)=A\cos(\theta)$ and taking inverse z transform arriving $y(n)=A\cos(n\theta)$. The implementation structure is showing in Fig.1 (b).

B. Algorithm for Multiple-output Digital Oscillator

From Fig.1 (a) and (b), we get following equation $y_2(n)=y(n-2)$. Take Z transform arrived

$$Y_2(Z)=Z^{-2}Y(Z)+Z^{-1}y(-1)+y(-2) ,$$

then arrange it can getting,

$$Y_2(Z)=[Z^{-1}\,y(-1) + (1-2\cos(\theta)\,Z^{-1}y(-2))] /(1-2\cos(\theta)Z^{-1}+Z^{-2}) \quad (6)$$

Combine Eq. (5), (6), if setting $y(-1)=0$,$y(-2)=-A$, getting ,

$$Y_1(Z)=AZ^{-1}/(1-2\cos(\theta)Z^{-1} + Z^{-2}) \quad (7)$$

$$Y_2(Z)=-A(1-2\cos(\theta))Z^{-1})/(1-2\cos(\theta))Z^{-1}+Z^{-2}) \quad (8)$$

If we multiply $\sin\theta$ to Eq.(7) at $y_1(n)$, then (7) becoming,

$$Y_1(Z)= A\sin\theta Z^{-1}/(1-2\cos(\theta)Z^{-1}+Z^{-2}) \quad (9)$$

Then take the inverse Z transform to (9), we arrive at $y_1(n)$ $A\sin(n\theta)$.

We get the sine signal wave output.

Next, combine Eq.s(7) and (8), if we multiply $\cos(\theta)$ to Eq.(7) at $y_1(n)$ and multiply negative 1 (-1) to Eq.(8) at $y_2(n)$, then by adding them, we get the following,

$$Y_1(Z)\cos(\theta) +Y_2(Z)(-1) = A(1-\cos(\theta)\,Z^{-1}) /1 -2\cos(\theta)Z^{-1} + Z^{-2} \quad (10)$$

Taking the inverse of Z transform of Eq.(10), we get $y_2(n)=A\cos(n\theta)$. So from the above algorithm we now obtain the ideal sin-cosine multiple-output oscillator. Obviously, real-time implementation that oscillator three multipliers are needed. Paper [2] proposed a modified oscillator which reduced the numbers of multipliers to 1 using following algorithm.

C. Modified Multiple-output Oscillator

For a fix-point oscillator with quantization step size is b, the coefficient $2\cos(\theta)$ is given as $2\cos(\theta)2^b= M$ .where M is integer, the bound of $2\cos(\theta)$ is [0 2], while the bound of M is $[1\ 2^{b+1}-1]$.

So we can get the bound of $2\cos(\theta)$ in fixed point implementation is summarized as. $2\cos(\theta)2^b=M$,and $2\cos(\theta)=M2^{-b}$.M=1,2,3, …$(2^{b+1}-1)$, The modified multiple-output oscillator is obtained by using the rounding to perform the quantization. The equations of modified multiple-output oscillator are given as,

$$\begin{aligned} y(n)&=2\cos(\theta)y(n-1)-y(n-2) ,\\ yc(n)&=-0.5\times 2\cos(\theta)ys(n)+ y(n) ,\\ ys(n)&=y(n-1) \end{aligned} \quad (11)$$

III. PROPOSED MULTIPLE-OUTPUT DIGITAL OSCILLATOR

The proposed oscillator utilized a second order error feedback network and a sign shift operation to reduce oscillator output roundoff error. Paper [10] introduced an implementation structure which reduced roundoff error remarkably. The proposed oscillator based on this structure is shown in Fig.2.

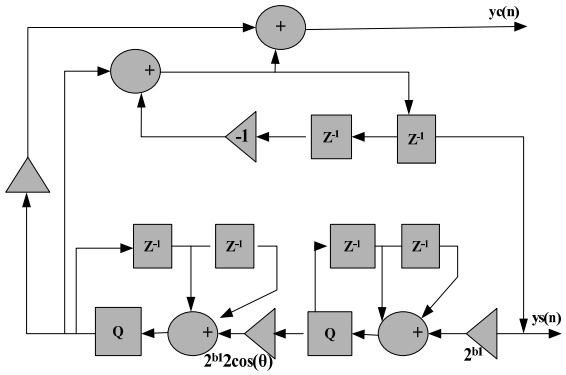

Fig.2 Modified multiple-output oscillator

The two second order error feedback networks in Fig.2 significantly reduce the frequency deviation through the finite word length limitation. The difference equation of Fig.2 is given below.

$$y(n)=Q_2\{Q_1[y(n-1)2^{-b1}–e_1(n-1)–e_1(n-2)] [2^{b1}2\cos(\theta)]- e_2(n-1)–e_2(n-2)\}- y(n-2) \quad (12)$$

By using Q[x] = x – e,

$$y(n)=2\cos(\theta)y(n–1)-y(n–2)–[e_1(n)+e_1(n-1)+e_1(n2)] [2^{b1}2\cos(\theta)]-[e_2(n)+e_2(n-1)+e_2(n-2 \quad (13)$$

Taking Z transform for Eq. (13), and set $y(-1) = e_1(-1) = e_1(-2)= e_2(-1) = e_2(-2) = 0$ and $y(-2) = -1$, then

$$Y(Z)=[A/1-2\cos(\theta Z^{-1}+Z^{-2}]–[E_1(Z)2^{b1}2\cos(\theta) + E_2(Z)](1+Z^{-1}+Z^{-2})/(1-2\cos(\theta)Z^{-1}+Z^{-2}) \quad (14)$$

Recall Eq. (14) where $\sin(\theta)=1$, for the frequency range of interest, and when Eq.s (9) and (10) are combined we get:

$$Y_s(Z)=(A\sin(\theta)Z^{-1}/1-2\cos(\theta)Z^{-1}+Z^{-2})–E_{sn}(Z)$$
$$Y_c(Z)=(A(1-\cos(\theta)Z^{-1})/1-2\cos(\theta)Z^{-1}+Z^{-2})–E_{cn}(Z)$$

where the term $A\sin\theta Z^{-1}/1-2\cos(\theta)Z^{-1}+Z^{-2}$and $A(1-\cos(\theta)Z^{-1})/1-2\cos(\theta)Z^{-1}+Z^{-2}$are the oscillator output sequences with quantization error in Z domain. The $E_{sn}(Z)$ and $E_{cn}(Z)$ are the effect of quantization noise output at terminals.

So, taking inverse Z transform for Eq. (11) ,we arrive $ys(n)=A\sin(n\theta)+e_s(n)$,$y_c(n)=A\cos(n\theta)+ e_c(n)$.The term $A\sin(n\theta)$ and $A\cos(n\theta)$ are the signals desired generation of oscillator while the term $e_s(n)$ and $e_c(n)$ are the noise components. The $e_s(n)$ and $e_c(n)$ are the additive components. Assume that the numbers represented in oscillator are two's complement and rounding operation is used for quantizing multiplier coefficients. So the input noise $e_1(n)$ with variance is given as $\sigma\, 2^{-2(b-b1)}/12$. The input noise $e_2(n)$ has a variance is $\sigma^2_2 =2^{-2b}/12$.

The variances of output roundoff error for oscillator are given which measure the error in K samples of the sinusoidal and cosinoidal of waveforms. If compared those roundoff errors with paper [10], it reduce the noise variance by about 9 times.

IV. THE COMPLETE OSCILLATOR STRUCTURE

This section introduce an extremely low frequency oscillator output sine sequence which used the trigonometric identities such as $\sin(\alpha-\beta)=\sin\alpha\cos\beta - \cos\alpha\sin\beta$. In this cases, we need to utilize two of the multiple-output oscillator to synthesize the generation of $\sin(\alpha-\beta)$. The figure of this oscillator structure is shown in Fig.3.

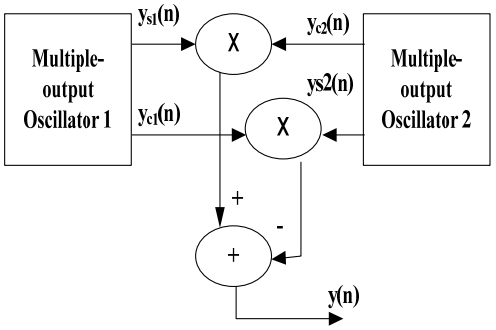

Fig.3 The complete oscillator structure

From Fig.3. it can be seen that each multiple-output oscillator can generate its own waves separately and independently. In other words, the amplitude and frequency of first oscillator output can be chosen independently from the second oscillator. The initial conditions for the first oscillator,

$y_1(-1)=y_2(-1)=0$, $y_1(-2)=-A$, $y_2(-2)=-B$. $y_1(-1)$,$y_1(-2)$ and $\theta_1 = 2\pi f_1/F$, as the same time $y_2(-1)$,$y_2(-2)$ and $\theta_2 = 2\pi f_2 / F$ are initial conditions of second oscillator.

$ys_1(n)=A\sin(n\theta_1)+e_{s1}(n)$,$y_{c1}(n)=A\cos(n\theta_1)+e_{c1}(n)$, $ys_2(n)=B\sin(n\theta_2)+e_{s2}(n)$,$y_{c2}(n)=B\cos(n\theta_2)+e_{c2}(n)$, Combined above Eq.s and using the trigonometric identities mentioned earlier, we obtain the output y(n) with the roundoff error as,

$$y(n)=[\sin(n\theta_1)+e_{s1}(n)[\cos(n\theta_2)+e_{c2}(n)]– [\sin(n\theta_2)+e_{s2}(n)][\cos(n\theta_1)+e_{c1}(n)]+e_1(n)+e_2(n)] \quad (16)$$

where the $e_1(n)$ and $e_2(n)$ are the output roundoff errors of proposed oscillator due to quantization after multiplication of first and second terms in Fig.3, respectively. The error $e_1(n)$ and $e_2(n)$ are small and can be ignored. This is a

consequence of the fact that $e_1(n)$ and $e_2(n)$ are not fed back into the system. Simplifying Eq. (19) the y(n) is given as,

$$y(n)=ABsin[n(\theta_1-\theta_2)]+e(n) \quad (17)$$

where the $ABsin[n(\theta_1-\theta_2)]$ is desired output sequences while e(n) is output roundoff error which can be obtained from (19) as,

$$e(n)=e_{s1}(n)cos(n\theta_2)+e_{c2}(n)sin(n\theta_1)+e_{s1}(n)e_{c2}(n) e_{s2}(n)cos(n\theta_1)-e_{c1}(n)sin(n\theta_2)-e_{c1}(n)e_{s2}(n) \quad (18)$$

From Eq.(17), it is clear that the output of presented oscillator is a sinusoidal sequence with $\theta=\theta_1-\theta_2$, $\theta=(2\pi f_1/F)-(2\pi f_2/F)=2\pi f/F$. So the output frequency $f=f_1-f_2$.

The sinusoidal term is given by

$$f_d=(\theta_1-\theta_2)F/2\pi \quad (19)$$

From above Eq. the number of samples per cycle of the generated sinusoidal is obtained as $N_s=2\pi/(\theta_1-\theta_2)=N_1N_2/(N_2-N_1)$,where:

$N_1=2\pi/\theta_1$, $N_2=2\pi/\theta_2$.

Eq.(19) has the smallest value when $\theta=\theta_1-\theta_2$ gives the smallest difference between θ_1 and θ_2 are coefficients of multipliers $2\cos(\theta_1)2^{b+1}=2M$ and $2\cos(\theta_2)2^b=2M$.

Hence the smallest value of θ which can be implemented by the proposed structure using b bits is given by $\theta_{min}=\theta_1-\theta_2$.

where θ_1 can obtain from $2\cos(\theta_1)2^{b+1}=2M$, $\theta_1=\cos^{-1}(M2^{-b-1})$ while θ_2 can obtain from $2\cos(\theta_2)2^b=2M$, $\theta_2=\cos^{-1}(M2^{-b})$.Then we expanding cos(θ) around the point $\theta=\pi/2$, using the Taylor expression

$$\cos(\theta)=\sin[(\pi/2)-\theta]=[(\pi/2)-\theta]-(1/3!)[(\pi/2)-\theta]^3+\ldots\approx[(\pi/2)-\theta] \quad (20)$$

So from Eq. (20), can arrives the following equation

$$2\cos(\theta_1)2^{(b+1)}=[(\pi/2)-\theta_1]2^{(b+1)}=2M,\quad \theta_1=(\pi/2)-M2^{(-b-1)} \quad (21)$$

$$2\cos(\theta_2)2^b=[(\pi/2)-\theta_2]2^b=2M,\quad \theta_2=(\pi/2)-M2^{(-b)} \quad (22)$$

Substituting Eq. (21) and (22) into $\theta_{min}=\theta_1-\theta_2$, can θ_{min} is obtained as.

$$\theta_{min}=(\pi/2)-M2^{-b-1}-[(\pi/2)-M2^{-b}]=M2^{-b-1} \quad (23)$$

The bound of M is given as as $1\le M\le 2^{b/2}-1$,we arrive $f_d=(M2^{(-b-1)}F)/2\pi$

and corresponding number of samples per cycle is $N_s=2\pi/M\,2^{(-b-1)}$.

In general, it is evident that the generated frequency is a linear function of M. The frequency difference between two adjacent frequencies (frequency resolution) is $2^{-b-1}/2\pi T$.

A. MATLAB Simulation Results

The frequency deviation Δfd (M) is a measure of the claimed uniform frequency spacing for oscillator and is defined as:

$$\triangle fd(M)=[fd(M)-Mfd(1)]/fd(1) \quad (24)$$

For the detail information to calculate the frequency deviation of proposed oscillator the readers are referred to the simulation results table. The total harmonic distortion (THD) is important characteristic to measure the performance of oscillator.

B. Definition of Total Harmonic Distortion Percentage

The total harmonic distortion determines the purity of a waves and is defined as,

THD=spurious harmonic power/Total waveform power=$(P_t-P(f_0))/P_t\times100\%$, where the spurious harmonic power is relates to the unwanted harmonic components of the waveform. P_t is the total power of sinusoidal waveform. $P(f_0)$ is the power of desired fundamental frequency f_0. P_t is the total power, which is related to N, where the N is the number of samples in the full period.

The results of simulation are obtained by assuming that the states y(n), y(n-1) and y(n-2) are represented using 11 bits fractional word length for sign and magnitude number representation in multiple-output oscillator1 and 10 bits in multiple-output oscillator2. The initial condition y(-2) is choose that y(-2)=-1. From $1\le M\le 2^{b/2}-1$, the bound of M is from 1 to $(2^{b/2}-1)$, [1 63].

TABLE 1. SIMULATION RESULTS

M	b_1	N_s	f_d(M) (kHz)	Δf_d (M) $\times10^2$	THD% $\times10^{-6}$	THD_p% $\times10^{-6}$
1	10	25,736	1.9428	0.0	5.389	5.086
2	9	12,868	3.8856	0.0	5.179	4.972
3	8	8578.6	5.8284	-0.5147	25.43	24.33
4	8	6434	7.7712	-0.5147	5.349	5.124
6	7	4289.3	11.657	-3.0883	25.99	24.85
10	7	2573.6	19.428	0.0	156.7	143.8
16	6	1609	31.09	2.0589	6.842	6.247
25	6	1029	48.570	-2.574	187.6	179.4
30	5	857.86	58.284	0.0	579	256.8
38	5	677.26	73.827	1.0294	361.4	340.7
43	4	598.5	83.541	-1.544	459.6	412.
51	4	504.63	99.083	-0.547	508.4	452.8
63	4	408.51	122.340	-1.544	584.8	519.2

The table given the value M which specifies the multiplier coefficient. The table also has given the sign

switching operation factor 2-b1 which is the input to the multiplier. The coefficient of multipliers required (11- b1) bits and (10-b1) to be implemented. The number of samples per cycle of generated sinusoidal signal, Ns is shown in table. The frequency of generation of proposed oscillator fd(M), and the frequency deviation ∆fd(M) are calculated by assuming the sampling frequency F is 50 MHz. The PHD% of proposed oscillator is compared with oscillator in [10]. Finally, the proposed oscillator is applied in a frequency-shift-keying (FSK) model and the result is shown in Fig.4.

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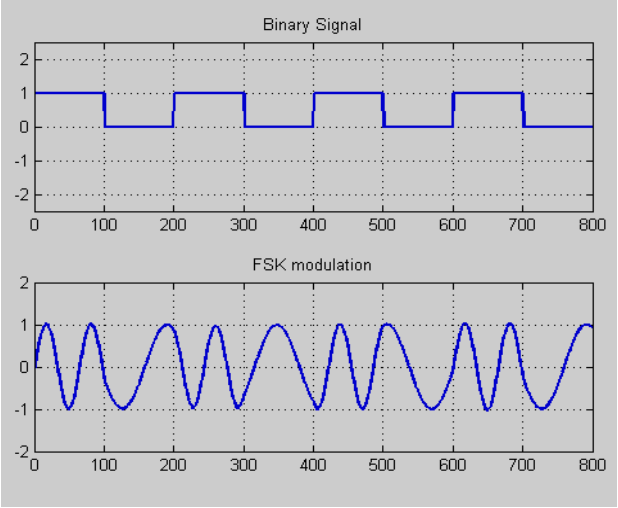

Fig.4 FSK application of proposed oscillator

Fig.4. shows the application of extremely low frequency oscillator with the output modulation signal phase is uniform and the amplitude is generated accordingly. So this proposed extremely low frequency oscillator is suitable to be applied in practical applications.

V. CONCLUSION

The proposed design shows the implementation of a low frequency digital sinusoidal oscillator structure generate very low frequency which employs two of multiple-output oscillator. It requires shorter word length bits multiplier for its hardware implementation than the other previously reported oscillator. The proposed oscillator structure generates much lower frequency compared with [10] while the disadvantage of proposed oscillator is requires one more multipliers if comparison to [10]. The advantage is that it obtains half low frequency than [10] during same conditions. The proposed oscillator has continuity phase and uniform frequency spacing which makes it suitable for telecommunication application such as radar, spread spectrum, frequency-division-multiplexing, and frequency shift keying (FSK).

CONFLICT OF INTEREST

The authors confirm that this article content has no conflicts of interest.

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