A High Resolution and Large Dynamic Range Capacitive Readout Circuit for Micro-Electromechanical System Accelerometer

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***Abstract* — This paper presents a low noise, high resolution and large dynamic range capacitive readout circuit for Micro-Electromechanical System accelerometer applying to seismic exploration. In comparison to conventional correlated double sampling structure, the proposed correlated double sampling structure is easier to realize, and the correlated double sampling capacitor in conventional structure is removed, also the number of switches is reduced to decrease switch thermal noise. The low frequency 1/f noise and offset voltage of op-amps are suppressed so as to improve resolution and increase dynamic range. The readout circuit chip has been fabricated using X-FAB 0.18-μm complementary metal-oxide-semiconductor technology, which measures 3.5mm^2. Test results show that the capacitive resolution of the readout circuit is 2.5aF and the dynamic range reaches 127dB with a sampling frequency of 128 kHz. The readout circuit achieves a noise floor of -115 $dBV/\sqrt{Hz}$ at 100Hz with a sensitivity of 0.71mV/fF.**

Keywords - digital geophone; MEMS accelerometer; capacitive readout circuit; correlated double sampling

I. INTRODUCTION

As the simple geological structure of oil/gas resources exploration is over basically, oil/gas resources exploration has entered a deeper and more complex geological structure. The cost of drilling increases in orders of magnitude, which requires higher resolution images for those difficult geological structure targets to reduce the risk of drilling. To achieve this, tens of thousands or millions of geophones with high sensitivity and broad bandwidth are needed to get dense sampling for the seismic reflective wave-field[1]. The core of Micro-Electromechanical System (MEMS) digital geophone is MEMS capacitive accelerometer that can directly convert acceleration of the ground motion to a digital signal. MEMS digital geophone with low power consumption and miniature size combined with mass production for itself and IC chip certainly can meet the geophone requirements for high density data collection, reliability and lower cost.

MEMS digital geophone is mainly composed of three parts: mechanical device, capacitive readout circuit chip and digital signal processing chip. This paper focuses on designing the capacitive readout circuit. The readout circuit of MEMS capacitive accelerometer is mainly divided into two categories: modulation-demodulation type[2] and switched capacitor type[3]. Modulation-demodulation readout circuits firstly modulate the acceleration signal to high frequency signal, and then the high frequency signal is amplified, finally the amplified signal is demodulated back to low frequency acceleration signal. In contrast to the modulation-demodulation type, the structure of switched capacitor readout circuits is simpler with no need for a demodulator. Besides, it has good stability and high precision. So switched capacitor readout circuit is adopted in this paper.

In order to meet the requirements of seismic exploration, such as high sensitivity, MEMS accelerometer has to try to reduce the noise within bandwidth of seismic signal. The noise of the readout circuit is the main noise source of accelerometer. The noise floor of the readout circuit is commonly -110 $dBV/\sqrt{Hz}$ [4, 5]. In order to further improve the accuracy of readout circuit, the design indicator of noise floor in this paper is -115 $dBV/\sqrt{Hz}$. At present, there are two basic techniques that are used to reduce the low-frequency noise of readout circuit, namely the auto-zero (AZ) and chopper stabilization (CHS) techniques[3, 6, 7]. The CHS technique is a modulation technique essentially. One disadvantage of this technique is the need for a high modulator and a low-pass filter. The correlated double sampling (CDS) technique is a particular case of AZ technique. The CDS technique was first used to filter out the reset noise of output signal of charge-coupled devices (CCD), and suppress low-frequency noise and broadband white noise[8]. It was later extended to switched capacitor circuit to suppress 1/f noise and offset of the input of op-amp or switch thermal noise of the output of op-amp. In contrast to the conventional CDS readout circuit[5, 9], the structure in this paper is simpler which reduces the CDS capacitor and the number of switches and suppresses 1/f noise and offset voltage effectively.

II. SYSTEM STRUCTURE AND OPERATING PRINCIPLE

A. Equivalent circuit of the mechanical device

The mechanical device of capacitive MEMS accelerometer is comprised of two fixed plate and a movable proof mass. Due to the effect of acceleration, the proof mass will move between the two fixed plates, and convert the acceleration into the variation of capacitance[10-12]. According to different types of the mechanical device, capacitive MEMS accelerometer can be divided into comb-drive type of in-plane movement and parallel plate sandwich type of out-plane movement. In comparison to comb-drive type, sandwich type has many advantages, such as larger proof mass, larger capacitance, higher resolution, etc. The sandwich type accelerometer in this paper uses 4-layer silicon fusion bonding. The proof mass weighs about 21mg. The measured results indicate that resonance frequency is 825Hz and quality factor is 58. The equivalent mechanical thermal noise (BNEA) is $27\,ng/\sqrt{Hz}$ by Eq. (5), which is far less than the noise level of readout circuit.

$$BNEA = \frac{1}{g}\sqrt{\frac{4k_B T\omega_0}{MQ}}[g/\sqrt{Hz}] \qquad (1)$$

where k_B is the Boltzmann constant, T is the Kelvin temperature, ω_0 is the resonance frequency, M is the mass of the proof mass, Q is the quality factor, g is the gravitational acceleration ($9.8 m/s^2$).

The structure of the mechanical device and equivalent circuit are shown in Fig.1. CT0 is the initial capacitor between the top plate and the center plate, CB0 is the initial capacitor between the bottom plate and the center plate, ΔC_T is the capacitance variation between the top plate and the center plate because of the displacement of the proof mass. ΔC_B is the capacitiance variation between the bottom plate and the center plate, and $C_T = C_{T0} + \Delta C_T$, $C_B = C_B + \Delta C_B$. When x<<d0, the difference between CT and CB is:

$$C_T - C_B = \varepsilon_0 \varepsilon A\left(\frac{1}{d_0 - x} - \frac{1}{d_0 + x}\right) \approx \frac{2\varepsilon_0 \varepsilon A x}{d_0^2} \qquad (2)$$

where x is the displacement of the center plate, d0 is the initial gap between the top plate and the center plate (The initial gap between the bottom plate and the center plate is same), ε_0 is vacuum permittivity, ε is relative dielectric constant, A is the area of the plate. From Eq. (1), it is noted that, when x<<d0, the displacement of proof mass is proportional to $C_T - C_B$, and they show a linear relationship.

(a) The structure of the mechanical device

(b) Equivalent circuit of the mechanical device

Fig.1 The structure and equivalent circuit of the mechanical device

B. System Structure and Operating Principle

The function of capacitive readout circuit is detecting the capacitance variation of capacitive sensor, and converting the capacitive signal to a voltage signal. Conventional capacitive readout circuit using CDS technique[5, 9] is presented in Fig.2. Its working principle is: when ϕ_1 =high and ϕ_2 =low, the CDS capacitor accumulates the offset and 1/f noise of the op-amp; when ϕ_1 =low and ϕ_2 =high, a new sample of the op-amp subtracts the signal on ϕ_1, as a result, a signal without offset and 1/f noise is got. However, the structure is relatively complex, and has many control switches introducing high switch thermal noise. The CDS technique in this paper has made up for the deficiency by removing the CDS capacitor and reducing the number of control switches.

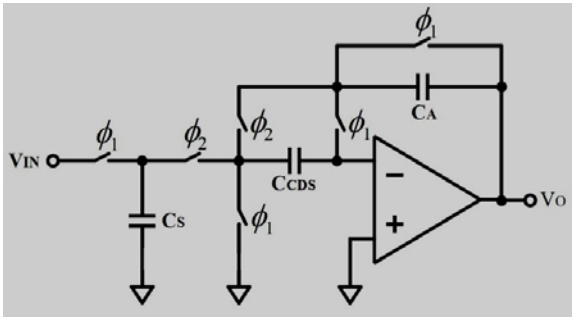


Fig.2 Conventional capacitive readout circuit using CDS technique

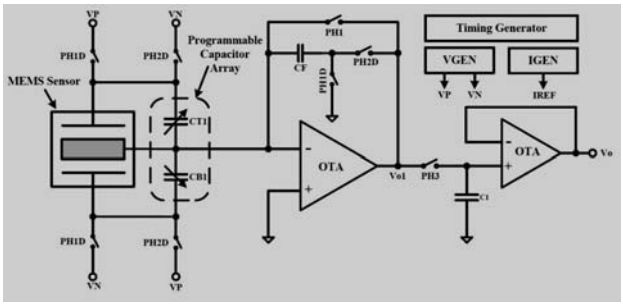


Fig.3 System structure of the capacitive readout circuit

The system structure of the capacitive readout circuit in this paper is plotted in Fig.3. It is composed of programmable capacitor array (PCA), analog front-end (AFE), sampling holder, timing generator, voltage and current reference. Capacitive sensing stage is controlled by two phase non-overlapping clock PH1 and PH2. When PH1=high, the top plate of sensor is connected to VP, the bottom plate is connected to VN, the left plate of feedback capacitor CF is connected to the inverting input of the amplifier, the right plate is connected to common mode voltage VCOM. The capacitor CF stores the offset and 1/f noise of the op-amp:

$$Q_T(PH1) = [VP - (V_{OS} + V_{COM})]C_T \tag{3}$$

$$Q_B(PH1) = [VN - (V_{OS} + V_{COM})]C_B \tag{4}$$

$$Q_F(PH1) = -V_{OS}C_F \tag{5}$$

When PH2=high, the top plate of sensor is connected to VN, the bottom plate is connected to VP, the charge on CT and CB is transferred to the feedback capacitor CF:

$$Q_T(PH2) = [VN - (V_{OS} + V_{COM})]C_T \tag{6}$$

$$Q_B(PH2) = [VP - (V_{OS} + V_{COM})]C_B \tag{7}$$

$$Q_F(PH2) = [V_{O1} - (V_{OS} + V_{COM})]C_F \tag{8}$$

According to the law of conservation of charge:

$$Q_T(PH1) + Q_B(PH1) + Q_F(PH1) = Q_T(PH2) + Q_B(PH2) + Q_F(PH2) \tag{9}$$

The output voltage of AFE is obtained as:

$$V_{O1} = (VP - VN)\frac{(C_T - C_B)}{C_F} + V_{COM} \tag{10}$$

where VOS is the offset voltage of op-amp, VCOM is the common mode voltage. As shown in Eq. (10), the offset of the op-amp is cancelled in the process. Combining Eqs. (2) and (10):

$$V_{O1} = (VP - VN)\frac{2\varepsilon_0 \varepsilon A x}{C_F d_0^2} + V_{COM} \tag{11}$$

Eq. (11) indicates that the displacement of the proof mass and the output voltage of the readout circuit have a linear relation.

From the results, the offset is eliminated. The CDS capacitor used in the conventional structure is taken out in this paper. The feedback capacitor CF can not only store offset and 1/f noise, but also be used as integrating capacitor. The output power spectral density (PSD) of the CDS circuit is equal to[9, 13]:

$$S_{OUT}(f) = 4\left(\frac{\sin(\pi f T_s)}{\pi f T_s}\right)^2 \times \sum_{n=-\infty}^{n=\infty} \frac{\sin\left(f - \frac{n}{T_s}\right)}{\beta^2}\left(\sin\left(\frac{\pi T_s\left(f - \frac{n}{T_s}\right)}{2}\right)\right)^2 \tag{12}$$

where Ts is the sampling period, β is the feedback factor of the amplifier, and Sin(f) is the input-referred PSD of the amplifier noise. Equation (12) shows that the input spectrum is multiplied by, $\sin^2(\pi T_s f/2)$ and 1/f noise is removed considerably.

The gain of the readout circuit can be obtained by Eq. (10):

$$k_{AFE} = \frac{V_{O1}}{\Delta C} = \frac{VP - VN}{C_F} = \frac{2V_{ref}}{C_F} \tag{13}$$

Where, $\Delta C = C_T - C_B$, VP-VN=2Vref. Assume $V_{O1,\max}$ is the maximum linear output voltage of AFE. The maximum input capacitance variation that the readout circuit can process is shown in Eq. (14)[14]:

$$\Delta C_{\max} = \frac{V_{O1,\max}}{k_{AFE}} \tag{14}$$

The minimum detectable input capacitance variation is:

$$\Delta C_{\min} = \sqrt{\frac{\overline{P}_N^2 \cdot BW_N}{k_{AFE}^2}} \tag{15}$$

where, $\overline{P_N}$ is the noise power spectral density (PSD) of $V_{O1,\,BWN}$ is the bandwidth of noise. As $\Delta C_{\min}$ is smaller, the capacitive resolution of the readout circuit is higher. Therefore, the capacitive resolution can be improved by reducing the output noise PSD or increasing the gain of the readout circuit. The dynamic range (DR) of the capacitive readout circuit is shown in Eq. (16). Increasing $\Delta C_{\max}$ or decreasing $\Delta C_{\min}$ would increase the dynamic range. Then, increasing $\Delta C_{\max}$ can be realized by increasing $V_{O1,\max}$ or decreasing k_{AFE}. But decreasing k_{AFE} would reduce the capacitive resolution. So, the most effective way to improve dynamic range is reducing the output noise level of the readout circuit.

$$DR = 20\lg(\frac{\Delta C_{\max}}{\Delta C_{\min}}) \tag{16}$$

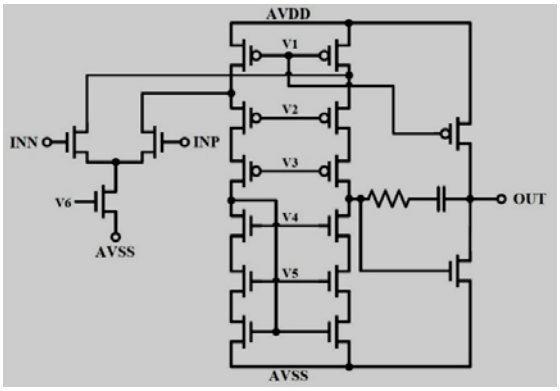
III. CIRCUIT DESIGN

A. Transconductance Amplifier

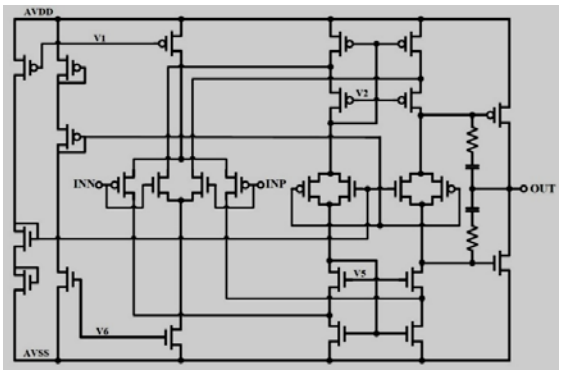
Generally, there are three kinds of topologies of op-amps: telescopic cascode op-amp, folder cascode op-amp, two stage op-amp. The speed of telescopic cascode op-amp is high, and the noise is low, but the output swings is limited and it is difficult to short the input and output. In contrast to telescopic cascode op-amp, the output swings of folder cascode op-amp is higher, but the gain is lower and the noise is higher. Two stage op-amp can provide both a high gain and a large swings.

The transconductance amplifier (OTA) of AFE needs to have high gain and large output swings, so a two-stage op-amp with miller compensation is adopted. Its schematic is presented in Fig.4 (a) (V1~V6 is provided by biasing circuit). The dc open-loop gain of the OTA is 114.4dB, the phase margin is 62.3°, and the unit gain bandwidth is 16.6MHz with 20pF capacitive load.

The OTA of sampling holder has to meet the requirement of high gain, full swings of the input and output, high drive capability. Therefore, a rail-to-rail two-stage op-amp is designed. Fig.4 (b) shows the schematic. The dc open-loop gain of the OTA reaches 135dB, the phase margin is 73.2°, and the unit gain bandwidth is 28.7MHz with 20pF capacitive load.



(a) OTA schematic of AFE



(b) Rail-to-rail OTA schematic of S/H

Fig.4 OTA schematic of AFE and S/H

B. Programmable Capacitor Array

When the mechanical device of accelerometer is fabricated, CT0 and CB0 have minor differences from each other because of processing deviation. Programmable capacitor array (PCA) is designed for compensating the deviation and other parasitic capacitances. PCA is a 8 bit capacitor array as plotted in Fig.5. The unit capacitance is 156fF, and the total capacitance is 39.936pF. TOP in Fig.5 connects to the top plate, BOT connects to the bottom plate and CTR connects to the center plate. There are totally nine groups of capacitors, and the capacitances of C1~C8 increase exponentially. The capacitor C0 connects to the bottom plate all the time. One plate of C1~C8 always connects to the center plate, and the other plate is controlled by the switches s0~s7 and s0b~s7b respectively. When s0~s7 are on, the capacitors connect to the top plate in parallel. Similarly, when s0b~s7b are on, the capacitors connect to the bottom plate in parallel. The capacitance variation range is -256C0~254C0.

PCA is used to simulate the capacitance variation of mechanical device as the input signal of AFE. The

relationship between input capacitive signal and output voltage signal of AFE is shown in Fig.6.

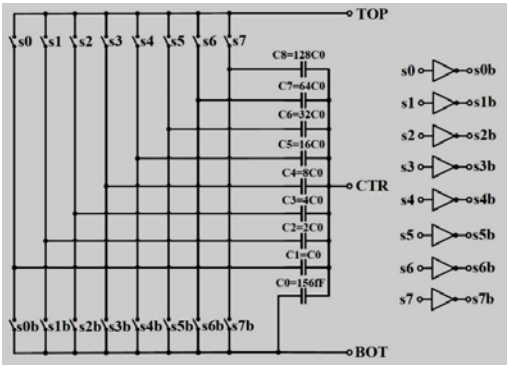


Fig.5 Schematic of PCA

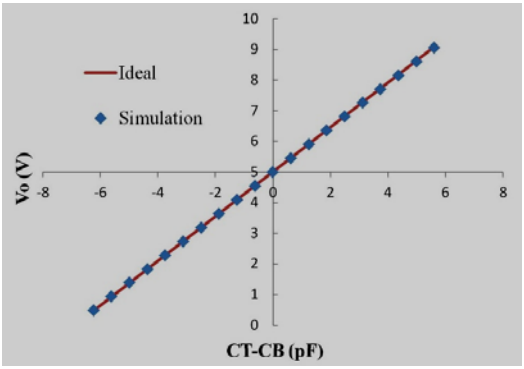
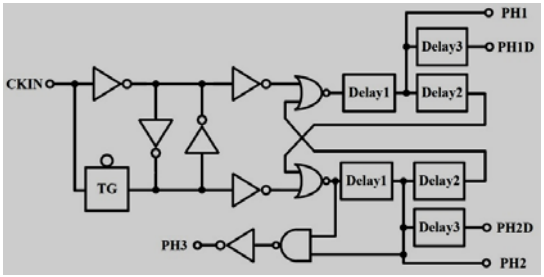


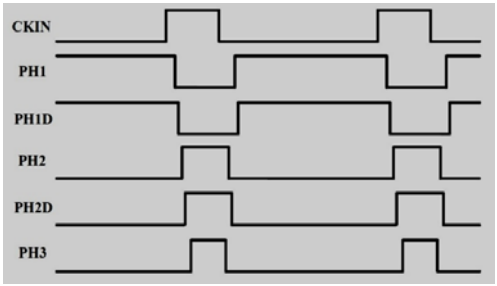
Fig.6 Simulated transfer curve of capacitor and voltage

C. Two-Phase Non-overlapping Clock Generator

In switched capacitor circuit, non-overlapping clocks are used to control capacitors charging and discharging. The schematic and timing sequence are presented in Fig.7. The non-overlapping clocks in this paper have two functions. Firstly, it is used to ensure that the charge is not lost. Secondly, the clocks can prevent the two reference voltages VP and VN from short-circuit. Dummy switches are used to minimize the problems of charge injection and clock feedthrough in the readout circuit.



(a) Schematic of two-phase non-overlapping clock

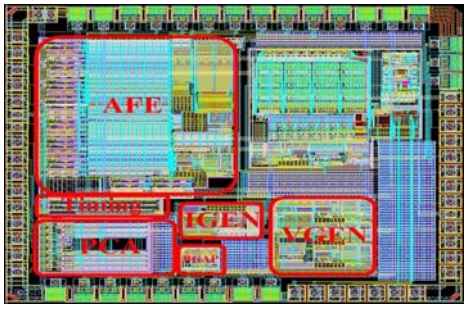


(b) Timing sequence of two-phase non-overlapping clock

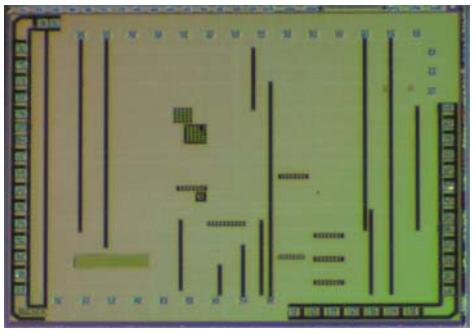
Fig.7 Schematic and timing sequence of two-phase non-overlapping clock

IV. TEST RESULTS

The readout circuit is fabricated with X-FAB 0.18μm 1P5M standard complementary metal oxide semiconductor (CMOS) process, which measures 3.5mm2 including analog front-end, programmable capacitor array, clock generator, bandgap, voltage reference and current reference. Fig.8 (a) shows the layout of the whole chip, and Fig.8 (b) presents the micrograph of the chip (The details cannot be displayed due to the top dummy metal layer). The sampling frequency of the circuit is 128 kHz, and the test result of two phase non-overlapping clock generator is shown in Fig.9.



(a)Layout of the capacitive readout circuit



(b) Micrograph of the chip

Fig.8 Layout and micrograph of the capacitive readout circuit

Fig.9 The test result of two phase non-overlapping clock

PCA is used to simulate the capacitance variation of mechanical device. The unit capacitance is 156fF, and the capacitance variation range is -39.936pF~39.624pF. Fig.10 plots the tested transfer curve of capacitance and voltage of the readout circuit and the test result shows that the sensitivity of the readout circuit is 0.71mV/fF. The noise test system of capacitive readout circuit and the output noise PSD of the capacitive readout circuit are given in Fig.11. The output noise floor is -115 $dBV/\sqrt{Hz}$ at 100Hz, the capacitive resolution is 2.5aF, and the dynamic range reaches 127dB. Table 1 shows the performance comparison results with other three types of circuits, including modulation-demodulation capacitive readout circuit, the capacitive readout circuit using CHS and the capacitive readout circuit using conventional CDS.

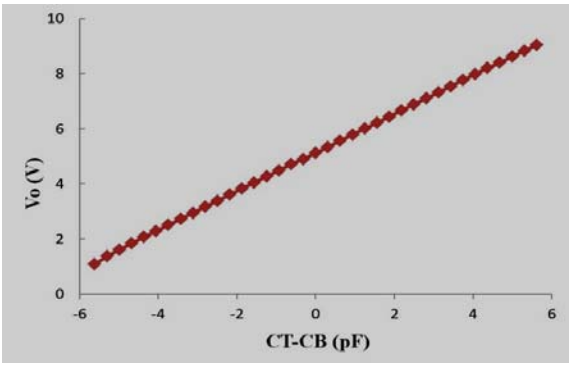
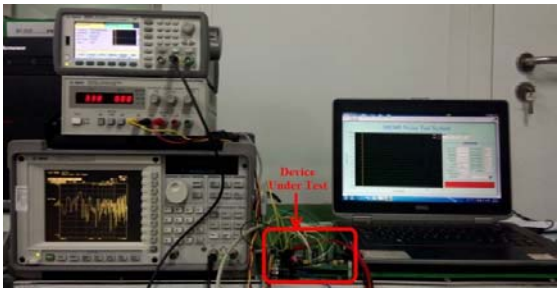
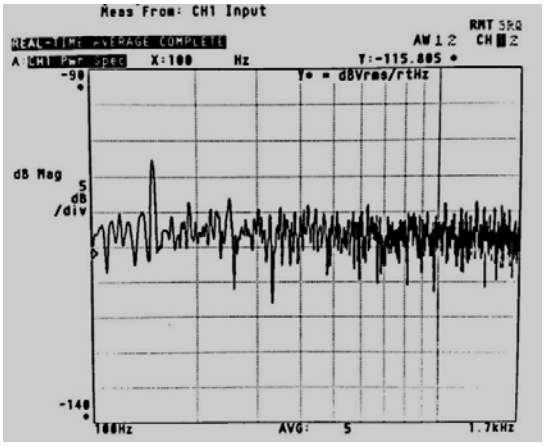


Fig.10 Tested transfer curve of capacitive and voltage of the readout circuit



(a) Noise test system of the capacitive readout circuit



(b) Noise power spectrum density of the capacitive readout circuit

Fig.11 Noise test system and the test result of the capacitive readout circuit

TABLE I. PERFORMANCE COMPARISON WITH THE REPORTED PAPERS

	[15]	[4]	[5]	This work
Resolution (aF)	—	50	1.5	2.5
Sensitivity (mV/fF)	0.25-80	0.56-13.3	1.67	0.71
Dynamic range (dB)	116	78.1	>100	127
Clock(kHz)	—	100	500	128
Process(μm)	0.5	0.35	0.35	0.18
Area(mm^2)	8.75	5	2.4	3.5
Structure	modulation	CHS	CDS	CDS

V. CONCLUSION

A high resolution, large dynamic range capacitive readout circuit using CDS technique for capacitive MEMS accelerometer is designed and realized in this paper. The CDS structure is simpler than the conventional one by removing the CDS capacitor and reducing the number of switches, which suppresses the offset and 1/f noise effectively. The capacitive readout circuit is implemented using 0.18μm CMOS process with an active area of 3.5mm2. Measured results indicate that the capacitive resolution of the readout circuit achieves as low as 2.5aF. The readout circuit reaches a noise floor of $-115\ dBV/\sqrt{Hz}$ at 100Hz with a sensitivity of 0.71mV/fF. The sampling clock runs at 128 kHz, and the dynamic range reaches 127dB

ACKNOWLEDGMENTS

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