LED Drive Power Optimization Design Based on Current Path

Shengwei Gao *, Qiang Li, Pingjuan Niu, Hong Wang, Xue Han, Xin Hao, Qiang Fan

Key Laboratory of Advanced Electrical Engineering and Energy Technology, Tianjin Polytechnic University, Tianjin 300387 China

***Abstract* — According to the existing LED drive power in pulse width modulation (PWM) dimming often appears to flicker, lower power factor, lower efficiency and other defects. By analyzing the working principle, current flow path, electromagnetic compatibility, the characteristic of power factor correction (PFC) of this kind of power, a circuit optimization design method and a device selection optimization design scheme have been proposed in view of the current distribution path of LED driver. Test results show that this scheme can achieve no flicker stable dimming of PWM from 0 to 100%. And power factor and efficiency are improved. In this paper, current path, device selection and electromagnetic compatibility factors are considered comprehensively. The influence of different circuit layout on the stability of the system is explored. The correctness of the optimized design scheme proposed in this paper is proved through tests.**

Keywords - Optimization design; Power factor; Current path; Electromagnetic compatibility; Dimming

I. INTRODUCTION

Energy crisis is always exist and will exist for a long time. We are trying to solve this problem. It has been our responsibility in every corner of the world to save energy. The annual energy consumption in lighting accounts for 40% -60%[1]. More energy will be saved if we take measures of energy saving in lighting. More energy-efficient LED lights have grown to become the preferred lighting in modern society. So, it has became a trend to design a dimmable and stability LED driver power.Now, the main problem is the flicker, low power factor and low efficiency happen when the PWM dimming has been applied in this type of power[2,3,4].

II.CIRCUIT WORKS AND CURRENT PATH ANALYSIS ANALYSIS

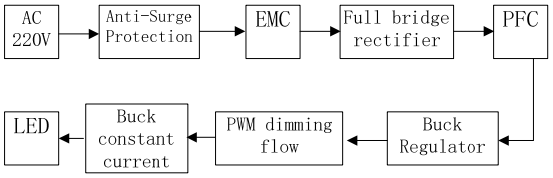


Fig.1 LED Drive System Function Diagram

The system function diagram has been shown in fig. 1. As is shown in fig.2, the main working part includes PFC, buck regulator, PWM dimming control, buck constant current. The black long arrow indicates current path[5,6].

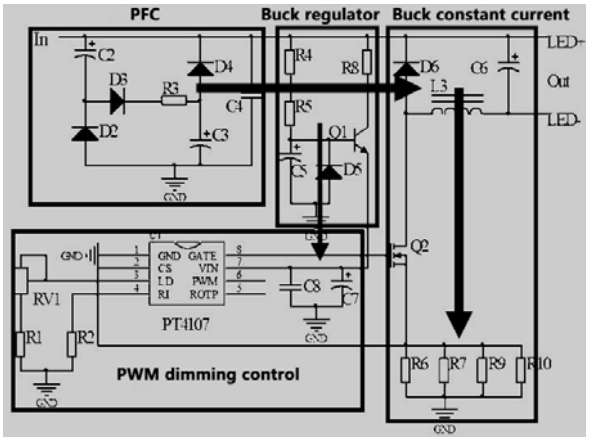


Fig.2 LED Driver Power Supply Circuit Diagram

A. PFC Design and Analysis

As is shown in fig.2, one arm of the half-bridge is constituted by C2 and D2, another arm of half-bridge is constituted by C3 and D3.Charging connection circuit consists of D4 and R3. The process of charged in series and parallel discharge can be achieved by using valley-fill principle. At the same time, the purpose of compensation for voltage is achieved[7,8,9].

When the capacitor line voltage is increased to half of the rated voltage of the capacitor, C2, D3, R3, and C3 are turned on. During the process, a series of charging circuit is turned on through the capacitor C2 and C3. Conversely, when the line voltage is decreased by half of the rated voltage of the capacitor, D2 and D4 will be forward biased. So, there will be two parallel roads to begin discharging[10,11]. Among them, C2 and D2 are connected in series, C3 and D4 are connected in series. Resistor R3 must be connected, there are three main roles: first, inrush

current on C2 and C3 of boot time can be limited, the effect of smooth the input current will be achieved; second, the function of suppress self-excited oscillation can be achieved; third, a better effect of the power factor can be achieved by limit the inflow current of capacitors C2 and C3. Based on the scheme proposed in this paper, the effect of smoothing can be achieved and power effect factor can be increased[12,13].

B. Capacitive Filtering Step-down Voltage Regulator Circuit

As is shown in fig.2, the buck regulator circuit consists of R4, R5, R8, C5, D5, Q1, it provide electricity for chip PT4107. Its effectiveness is called power purifier. There are two main functions in the circuit, including low-pass filter capacitor multiplier and series regulator. The electrolytic capacitor C5 is connected between the base and the ground[14,15,16]. The results with the ratio of the base current and the emitter current can be calculated as formula 1:

$$n=\frac{I_{emitter}}{I_{base}}=(1+\beta) \tag{1}$$

It is equivalent to a n times of the C4 capacitance between the emitter and ground in fig. 4. D5 is a 18V zener diode, and R4 and R5 are connected in series to form a series regulator. High-frequency switching ripple can be effectively eliminated through this circuit.

C . Buck Constant Current Circuit

As is shown in fig.2, the buck and the constant current circuit are consist of a series of devices, including control chip U1, fast recover diode D6, the inductor L3, power MOS Q2 and parallel to R6, R7, R9, R10, adjust resistor R1 and RV1, FM resistor R2[17].

The peak current is acquired U1 to the control chip, through the sampling resistor R6, R7, R9 and R10. After the internal logic of U1, the duty cycle of the PWM wave output of U1 GATE port is controlled. The purpose of constant current control can be achieved. Based on the freewheeling circuit which consists of D4 and L3, load of the LED lamp can be provided power of a constant current. The upper limit of the output current by controlling the magnitude of the resistance RV1 is set so that the load to obtain a different upper-limit current value. Due to the output current can be adjusted automatically through the port of CS in U1, the peak current can be collected. The size of the output of constant current can be determined by setting the sampling resistance size[18,19].

In different input and output conditions, the peak current will be automatically changed to obtain a stable output current[20]. The size of peak current is calculated as formula 2:

$$I_P^* = \frac{V_{ref\_cs}}{R_{cs}} + I_{pd} \tag{2}$$

In formula 2, V_{ref_cs} can be expressed in formula 3.

$$V_{ref\_cs}=V_{ref}\times(1+0.8\times D)\left(\frac{V_{IN}-V_{DD}}{R2+R3}-I_{DD}\right) \tag{3}$$

In the upper formation, I_P^* is the collected peak current; V_{ref} = 275mV; D is the duty cycle of the PWM wave of GATE output port in U1. It can be expressed in formula 4;

$$D=\frac{t_{ON}}{t_{OFF}+t_{OFF}} \tag{4}$$

V_{IN} is the DC Voltage after rectified; VDD is the base voltage of Q1, which is 18V; IDD is the operating current, the current size is determined by the operating frequency and Q1; R_{cs} is the equivalent resistances with four sampling resistors; I_{pd} is the additional current which exists because of the delay. In this circuit, there are four volumes which are constant, including the input voltage, output voltage, R2 and R3. I_{pd} is very small,low volatility, and negligible. For these reasons, after selecting Q2, in order to change the upper limit of the output current, it is necessary to change the operating frequency. There are two factors which affect the frequency of the chip GATE port output PWM waveform: the resistance size of R2 and the size of peak current collected by CS port. Since the size of the frequency setting resistor R2 has been limited,when the frequency setting resistor reaches the limit, the method which change the size of sampling resistor will be used to change the output current limit. It is the only way to effectively change the upper limit of the output current. However, in order to output a constant current for a long time stably, D4 and L3 must have a corresponding change, an effect of fit will be achieved[21].

There are some problems in this kind of power, such as dispersion and electromagnetic device compatibility issues. These factors will lead to production out of every piece of the output current of the power board will be slightly different. In this case, each power board output current can be adjusted by RV1. To change this situation, RV1 has been designed in the LI port. To ensure the stability of the modulated power board, be sure to use a turbine vortex rod trimmer potentiometer, and must add solid seal.

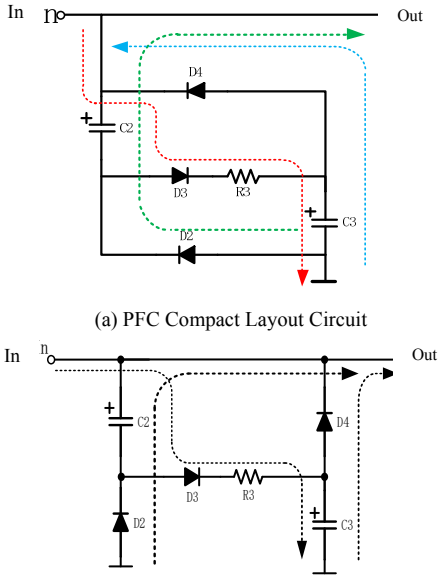
III. DESIGN AND OPTIMIZATION OF THE KEY POINT BASED ON CURRENT PATH

Current path has an important effect on the stability of the power system. It can directly determine the two important factors. One is the management of EMC and the other is the device selection.

A. PFC current analysis and circuit layout

The voltage waveform can be smoother than no PFC and the power factor of the circuit can be improved by the

addition of PFC circuit. The circuit layout of PFC is essential. The unreasonable layout of the PFC can eventually lead to affecting the stability of the circuit.



(a) PFC Compact Layout Circuit

(b) PFC Optimized Layout Circuit

Fig.3 PFC Circuit Layout

In fig.3, there are two different layouts of the PFC circuit board comparison chart. The dotted line in fig.3 indicates the current charge and discharge path.

As is shown in fig.3(a), the layout of PFC which place three diodes horizontally cannot achieve the function of PFC. Not only the power factor has not been improved, but also the noise in the circuit which has been increased and can eventually lead to generate the interference. As is shown in fig.3(b), the layout of PFC which place three diodes vertically can achieve the function of PFC. The power factor has been increased to the maximum by placing three diodes vertically.

B. Electromagnetic Compatibility Analysis

In terms of electromagnetic compatibility, it is very important that the layout of the device and the circuit plan in making Printed Circuit Board (PCB).

In planning the layout of the device, when the requirement of safety distance has been meeting, the device could be placed to achieve the purpose of convenient wiring. In addition, the device must be placed to reduce the length in parallel of the high-speed lines. Two or more high-speed lines which have long parallel wiring may produce unexpected inductance.

The self-excited oscillation which has been caused by the induction inductance can eventually lead to burning of the circuit board.The ground has been routed around the high-frequency circuit for better protection for high-frequency signal.

The circuit GATE port has been connected to the power transistor G port of Q2, whose output of the PWM signal is 25 KHz to 300 KHz. The lines of neighboring should be tried to keep vertical and by the ground circuit routing around this line,so the purpose of reducing electromagnetic interference can be achieved.

C. Device Selection and Optimization Design

In device selection, the most important thing is to choose a properly rated voltage and rated current of the devices. In normal operation state of the power, no-load and full load must be taken into account. There are some devices to withstand 311V voltage, such as D3, C4. At the same time, the circuit instantaneous starting voltage fluctuations must also be taken into account. Therefore, the rated voltage of the device must be greater than 311V.

The charge of capacitor has been considered to be the main reason for the generation of the inrush current at start. In order to effectively remove harmful inrush current, the thermistor of NTC must be connected to AC side when turn on the circuit. So safety and stability of the circuit can be increased greatly. But the choice of thermistor is crucial. The raring of thermistor is too small to bear the inrush current. On the contrary, the rating of thermistor is too big to lead to cost increas. So we must try to reduce the resistance of NTC within a reasonable range. According to the experience, the resistance of thermistor can suppress the current about five times than the normal work when input the maximum voltage. The resistance of the thermistor derived formula is as formula 5,6,7 :

$$V_b = 1.5 \times (\sqrt{2} \times V_{AC\max}) \tag{5}$$

$$I_b = \frac{I_O}{\eta} \tag{6}$$

$$R_{NTC} = \frac{V_b}{5 \times I_b} \tag{7}$$

In the upper formation, V_b is rated voltage of rectifier bridge; $V_{AC\max}$ is the maximum value of the input AC voltage; I_b is rated current rectifier bridge; Io is the size of output current; η is the efficiency of the circuit; R_{NTC} is thermistor resistance. Fuse F1 is connected to AC side to prevent circuit breakdown of over current. In this circuit, there are three conditions must be met for the inductor L3. First, the rated current of the inductor L3 must reach to 0.5A, so it cannot be burned when the circuit in the event of the short circuit; second, the winding resistance of the inductor must be less than 2 Ω ; Last but not the least, temperature resistance must be greater than the Curie temperature of 40 degrees.

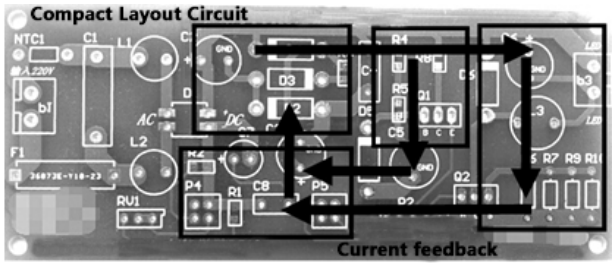
In the selection of device, frequency is the second thing that must be considered into.Q2 is the only high-frequency device in this circuit. The output frequency of the GATE port of the U1 range from 25 KHz to 300 KHz. The operating frequency of U1 can be calculated as formula 8:

$$F_{OSC}=\frac{30000}{R2[K\Omega]}[KHz] \quad (8)$$

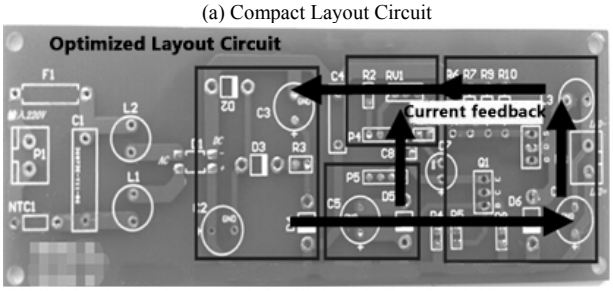
In the upper formation, R2 = 477K Ω, the GATE port output frequency FOSC = 62.88 KHz. Therefore, frequency of the switch must be greater than 63 KHz of Q2.

IV.EXPERIMENTAL DATA AND RESULTS ANALYSIS

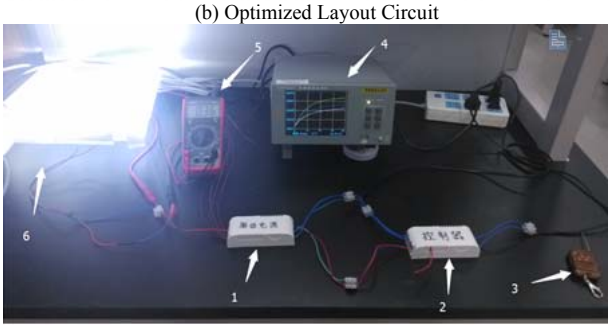
A. Experimental Method



(a) Compact Layout Circuit



(b) Optimized Layout Circuit



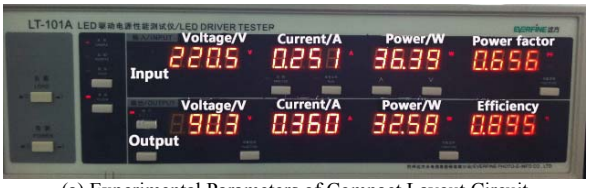
(c) System Test

Fig.4 System test graph

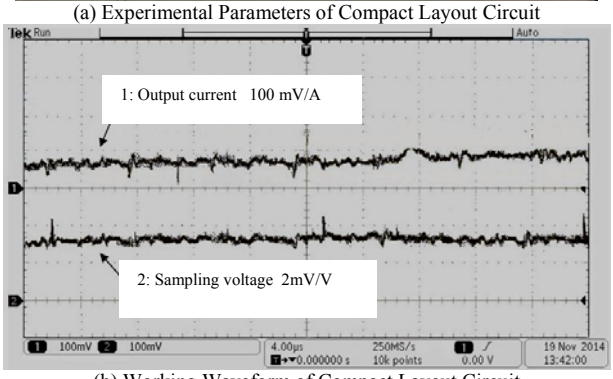
In fig.4 : 1.LED power driver; 2.Power supply PWM controller; 3.Power remote controller; 4.Test instrument; 5.Ammeter; 6.LED lamp load.

Based on the above analysis, experimental tests have been performed. The experimental conditions: input 220V AC voltage, the load is 32 W total power lamp boards. The experimental system is shown in fig.6. Two circuit structures have been tested in fig.4(a) and fig.4(b). The two circuits can work normally, but the different layout lead to different working parameters. The test experiment has been shown in fig .4(c).

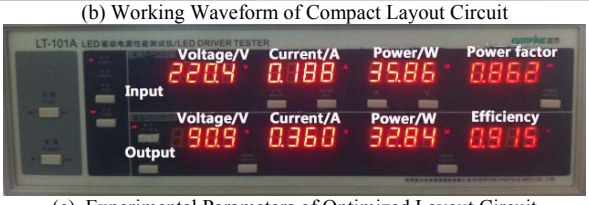
B. Analysis of The Influence Factors of Output Current



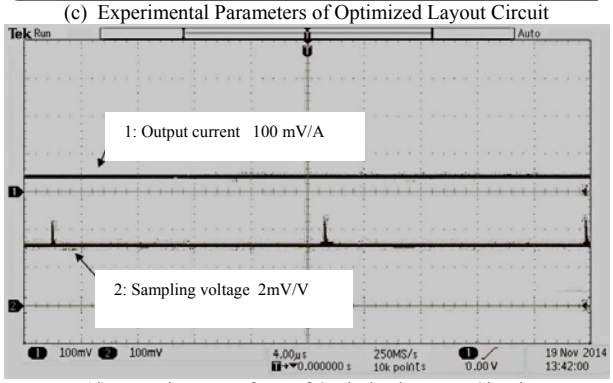
(a) Experimental Parameters of Compact Layout Circuit



(b) Working Waveform of Compact Layout Circuit



(c) Experimental Parameters of Optimized Layout Circuit



(d).Detection Waveform of Optimized Layout Circuit

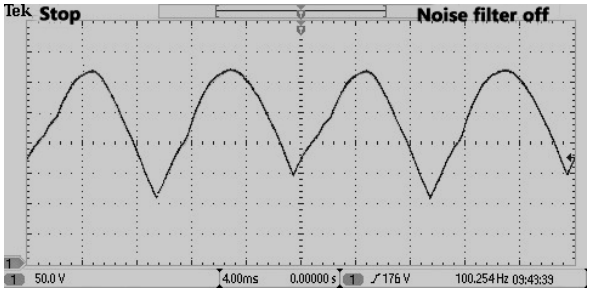
Fig.5 Measure Data Graph

The fig.5(a) and fig.5(b) are the experimental parameters and detection waveform about the compact layout circuit. It can be seen that the efficiency and power factor in fig.5(a) is significantly lower than that is in fig.5(c). The main reason is that waveform quality of the output current and sampling voltage in fig.5(b) is worse than that is in fig.5(d).

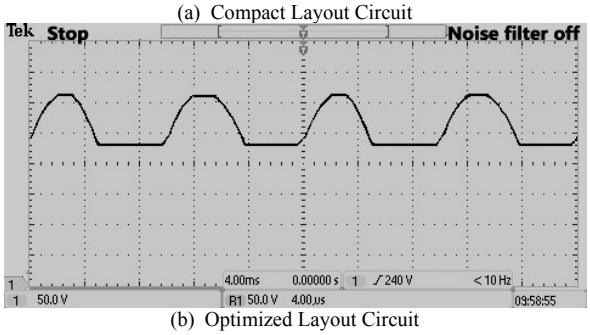
The fig.5(c) and 5(d) are the experimental parameters and detection waveform about the optimized layout circuit. In fig. 5(c) , it is the input and output power parameters. When input voltage is 220V AC and PWM control port is vacant, the current fluctuations kept below 10mA. At this time, the output voltage of the drive power was kept in a very stable state and the fluctuation rate of output voltage was below 5%. The power factor of driving power was kept at 0.86 or more. Efficiency was above 91% level. The fig.5 (d) is the

waveform of the output voltage. As is shown in fig.5 (d), the output of DC voltage of 90V was very stable.

The PFC circuits of different layouts have been tested. The test parameters and waveform obtained are shown in fig. 6.



(a) Compact Layout Circuit



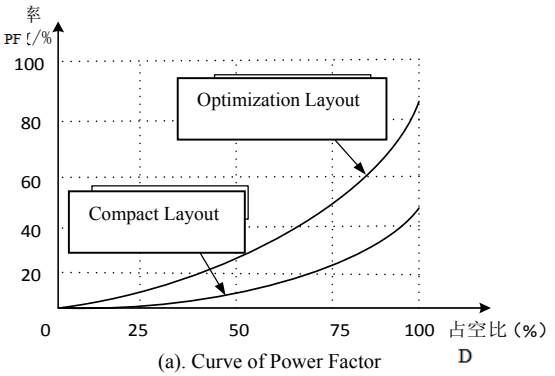
(b) Optimized Layout Circuit

Fig .6 PFC Layout Results Comparison Graph

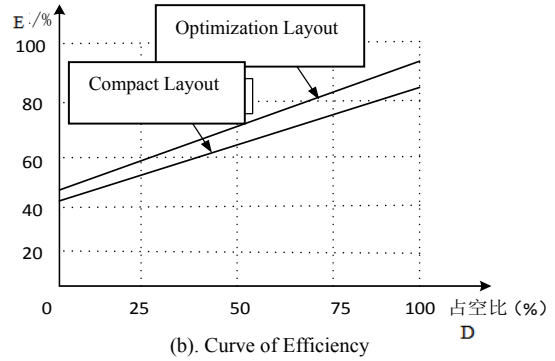
Fig.6(a) and fig.6(b) are the testing results of the two different layout circuits in fig.3(a) and fig.3(b). The two waveform diagram of voltages in Fig.6 has been collected at "out" point in fig.5(a) and fig.5(b). By comparison, the voltage, current, and power are almost same in both cases. But the power factor and efficiency of fig.5(a) were much lower than fig.5(c). As is shown in fig.6(a), the waveform of the voltage is not regular. Circuit stability was greatly reduced by the layout of PFC. While in fig.6(b), the waveform of the voltage is very normal. So the layout of PFC played a significant role in improving the power factor. The results also demonstrated that the impact of PFC circuit layout for the circuit power factor and stability.

C. Comparison And Analysis of Comprehensive Performance

High-precision wave controller of PWM has been made to test this drive power. The output frequency of this controller has been fixed at 800 Hz, but the duty cycle of this controller can be adjusted from 0 to 100%. After the input voltage and load has been fixed, the drive power supply output current was linearly adjusted by adjusting the duty cycle of the controller. When the duty cycle was adjusted to 100% and 0%. The output current of power supply changed linearly from 0 to 0.36A when the duty cycle of PWM wave was adjusted from 0 to 100%. And it remained stable in the two extreme cases. The Power, power factor and efficiency were critical parameters in the process of adjusting the current. In this circuit, the power was basically unchanged and the power factor was maintained above 0.86. The efficiency increased as the duty cycle increased. The maximum efficiency is more than 91% . Working performance dynamic comparison is in fig. 7.



(a). Curve of Power Factor



(b). Curve of Efficiency

Fig.7 Analysis of Experimental Result

Comparison of the final parameters of two circuits is in the Table I. As it was shown, the output voltage, current, power meet rated design requirements in the circuit of test , but the optimization layout circuit has higher performance. The main reason lies in the power supply design in the process of considering current path, optimize the layout and reduce the current path redundancy and electromagnetic interference.

TABLE I. THE PARAMETERS COMPARISON IN DIFFERENT LAYOUT

Test condition	Compact layout circuit	Optimized layout circuit	Unit
Input current(I_{in})	251	184	mA
Input power(P_{in})	40.1	38.6	W
Power factor(PF)	0.656	0.864	PF
Output voltage(V_{out})	96.4	97.8	V
Output current(I_{out})	360	360	mA
Output power(P_{out})	34.7	35.2	W
Efficiency(E)	86.5	91.1	%

Through the above analysis, it can be seen that the optimized layout circuit in the power factor and efficiency is significantly higher than the compact layout circuit, so it is very important that fully consider the current path in the power circuit design process.

V. CONCLUSION

In this paper, the design ideas and working principles based on the LED power current path circuit have been explained in detail through theoretical analysis. Feasibility of this circuit has been tested by experiment. In terms of current path, after careful analysis, the stable performance of the PCB has been produced. Problems of the PFC layout have been discovered and solved by experimental analysis. So the power factor of the circuit has been improved effectively. Based on the experimental data of the waveform and temperature, the reliability of the circuit optimization design method based on current path has been verified effectively.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflicts of interest.

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