Low Power Balun-LNA for Subsampling Architecture of Receiver

Fanzhen Meng[1,2], Hong Liu[1] ,Mingliang Wang[1], Tong Tian[1,2*]

[1]Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai, China
[2]University of Chinese Academy of Sciences, Beijing, China

Abstract — **A single-ended-to-differential conversion balun-LNA is proposed in this paper for subsampling architecture of receiver. The LNA adopts the inductively degenerated common-source common-gate (cascade) structure with noise canceling technique, which can achieve high gain and low noise figure without extra components and power consumption. For the subsampling receiver of IoT narrowband application, the LNA is integrated in 65 nm CMOS. It can achieve a noise figure of 1.5dB at the 780MHz, a differential voltage gain of 30 dB and gain and phase mismatch within 0.5 dB and 5o in the range from 775MHz to 785MHz, which is adequate for most of IoT applications. The proposed LNA consumes about 1.6mA with 1.2 V voltage supply.**

Keywords - Subsampling receiver; Balun-LNA; 780MHz IoT; low power

I. INTRODUCTION

With the increasing requirements for wireless communication of Internet of Things, we pay more attention on the performance, such as high integration, low power, low cost and multi-mode [1,2,3]. In order to meet the above performance, low power subsampling architecture of receiver should be used [4]. Low-noise amplifier (LNA) as the first block in the receiving chain is of great importance. Its voltage gain, noise figure and power consumption can affect the performance of the whole system [5,6,7].

Usually, the common-source common-gate (cascode) structure could be widely used for LNA design [8,9,10]. Common-gate (CG) topology can easily eliminate miller effect and common-source (CS) can acquire high voltage gain. For example, the inductively degenerated cascode configured LNA exhibits high gain and low noise figure, as shown (Fig. 1 (a)) [11]. In order to restrain the common mode noise and reduce parasitic couplings, the single-ended LNA should be converted to differential output. Generally, the off-chip baluns could be used to achieve differential signal. Although the off-chip baluns decrease the complexity of the system and the performance is better, it sacrifices the size and integration level. Fortunately, the noise-cancelling differential configuration LNA has been reported as shown (Fig. 1 (b)) [12,13,14]. For example, an inductorless low-noise amplifier (LNA) with the active balun can achieve with 15 dB gain and NF of 3.5 dB with gain and phase errors below 0.3 dB and 2 degrees [14].
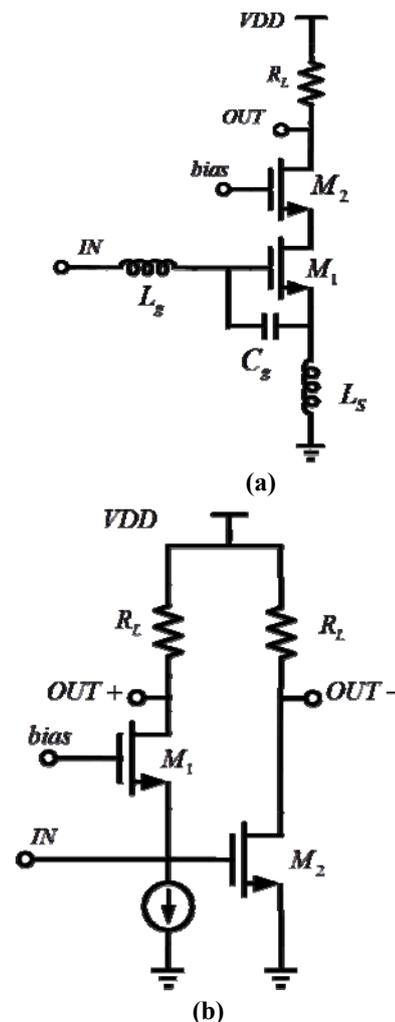

(a)

(b)

Fig.1(a) Schematic of the Inductively Degenerated Cascode Configured LNA and (b) the Noise-Cancelling Differential Configuration LNA

Although the CG-CS differential structure can achieve high voltage gain and generate the differential signal of phase opposite and equal amplitude, which is very sensible to the process variation [13]. Considering the advantages of the inductively degenerated cascode and the noise-cancelling differential configuration, new balun-LNA is reported in [11,15]. The balun-LNA consumes only 2 mA current from a 1.8 V supply and exhibits a differential voltage gain of 30.4 dB and a noise figure of 1.8 dB [15]. However, large inductor L increases size of the chip. Otherwise, lower supply voltage of MOS transistor with the new CMOS process technology, such as in the weak inversion (WI) or moderate inversion (MI) region, can make power consumption further reduced [16,17], such as in the MI–WI region, the power consumption of the LNA is only 0.68mW [17].

In the paper, the inductively degenerated balun-LNA with the noise canceling technique is proposed in Section II. Architecture and analysis of the balun-LNA are introduced in Section III. Circuits design and the performance of the balun-LNA will be exhibited in Section IV. Finally, the conclusions and discussion are drawn in Section V.

II. ARCHITECTURE AND ANALYSIS OF PROPOSED LNA

A. *Architecture of LNA*

The proposed balun-LNA is shown (Fig. 2), based on inductively degenerated cascode differential configuration. The RF signal coming from antenna is amplified by LNA. Firstly, transistors M1 and M2 consisting of the cascode topology could achieve high gain and input impeding matching, with the inductors Ls, Lg and capacitor Cg. And then transistors M3 and M4 consisting of the common-gate and common-source differential topology can provide the noise canceling and distortion canceling. The single-ended RF signal is transferred from the drain of M2 to the source of M3 and the gate of M4 through the capacitor C_c for differential output. Capacitor C_b provides the AC coupling to ground and bias supply voltage makes enough current differential output, which avoids using the larger inductor L coupling to DC current. The sizes of M3 and M4 should meet the proper proportion for acquiring the signal of equal amplitude and opposite phase. In addition, the larger resistor R_{CG} and R_{CS} could be used to achieve high voltage gain.
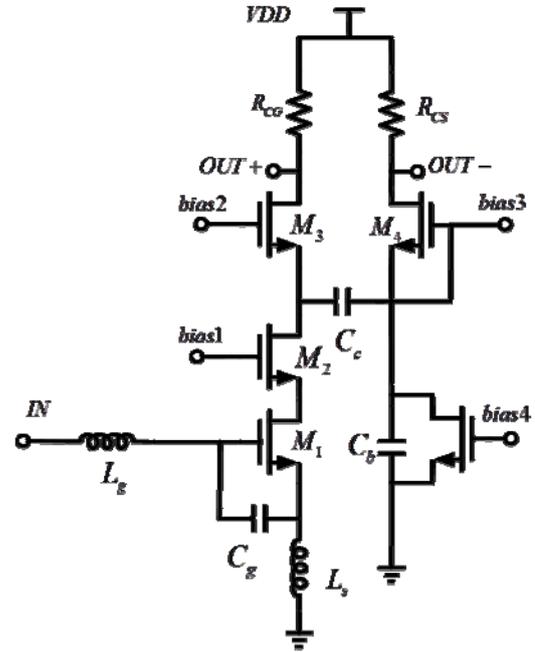

Fig.2 Schematic of the Proposed Balun-LNA

B. *Input Matching*

The input impedance matching of the balun-LNA can easily achieve with the inductively degenerated inductors L_s, input impedance of Z_{in} can be expressed as [9],

$$Z_{in} = jw(L_s + L_g) + \frac{1}{jw(C_{gs} + C_g)} + \frac{g_{m1}L_s}{(C_{gs} + C_g)} \quad (1)$$

where g_{m1} is the trans-conductance of M1 and C_{gs} is the gate-source capacitance. From (1), the source degenerative inductor Ls can easily achieve the real matching without generating extra noises, and capacitor C_g could relax the constraint of power consumption. When input impedance of Z_{in} is matched to 50Ω, thus: Re[Z_{in}] = 50 Ω and Im[Z_{in}]. The resonance frequency w can be expressed as,

$$w = 1 \Big/ \sqrt{(L_s + L_g) \square (C_{gs} + C_g)} \quad (2)$$

C. *Noise Analysis*

In order to analyze the noise figure of the balun-LNA in detail, noise figure of every stage would be listed respectively. Firstly, regardless of the noise contribution from the cascade stage M2, the noise figure NF1of M1 can be calculated as [10, 18],

$$NF1 = 1 + \frac{2}{\sqrt{5}} \square \frac{w(C_{gs1} + C_g)}{g_{m1}} \square \sqrt{\gamma\delta(1 - |c|^2)} \quad (3)$$

where the $\gamma,\ \delta,\ c$ are process parameter. NF1 is determined by the trans-conductance gm1 of M1 and the gate-source capacitance C_{gs1} and capacitor C_g.

Secondly, the typical CG–CS topology is widely used, which has been analyzed in detail [14]. The noise figure NF2 of the CG–CS topology can be calculated as,

$$NF2 = 1 + \frac{\gamma g_{m,CG} \square \left(R_{CG} - R_S \square g_{m,CS} \square R_{CS} \right)^2}{R_S \square A^2_{V,2}} +$$

$$\frac{\gamma g_{m,CS} \square R^2_{CS} \square \left(1 + g_{m,CG} \square R_S \right)^2}{R_S \square A^2_{V,2}} + \qquad (4)$$

$$\frac{\left(R_{CG} + R_{CS} \right) \square \left(1 + g_{m,CG} \square R_S \right)^2}{R_S \square A^2_{V,2}}$$

where the second part and the third part are respectively the noise contribution from the CG transistor M3 and CS transistor M4, and the last part from the load. The voltage gain $A_{V,2}$ of differential configuration can be expressed as [13],

$$A_{V,2} = g_{m,CG} \square R_{CG} + g_{m,CS} \square R_{CS} \qquad (5)$$

where $g_{m,CG}$ is the trans-conductance of M3, $g_{m,CS}$ is the trans-conductance of M4, R_{CG} and R_{CS} are respectively the load resistance from M3 and M4 , and R_s is output resistance of M2.

The noise figure NF2 of the CG–CS topology would be further analyzed by simulation, assuming that the trans-conductance $g_{m,CS}$ is n times bigger than the trans-conductance $g_{m,CG}$ and the load resistors R_{CG} is n times bigger than the load resistors R_{CS}. When CG transistor M3 is matched, R_S is the reciprocal of trans-conductance $g_{m,CG}$ ($R_S = 1/g_{m,CG}$) Therefore, the noise figure and voltage gain of CG–CS topology can be respectively rewritten as (6) and (7),

$$NF2 = 1 + \frac{4\gamma g_{m,CG} \square \frac{R^2_{CG}}{n}}{R_S \square A^2_V} + \frac{4\left(1 + \frac{1}{n}\right)R_{CG}}{R_S \square A^2_V} \qquad (6)$$

$$A_{V,2} = 2 g_{m,CG} \square R_{CG} \qquad (7)$$

From (6), NF2 is determined by the trans-conductance $g_{m,CG}$ of M3 and the load resistors R_{CG}. Because of the matching condition, the trans-conductance $g_{m,CG}$ is 20mS and R_S is50Ω. γ is about 4/3, and the load resistors RCG is about $1000\,\Omega$ for high voltage gain. Noise figure NF2 of the CG-CS topology is clearly shown (Fig. 3), which noise figure NF2 would become smaller by increasing ratio n (*n* = $g_{m,CS} / g_{m,CG}$).
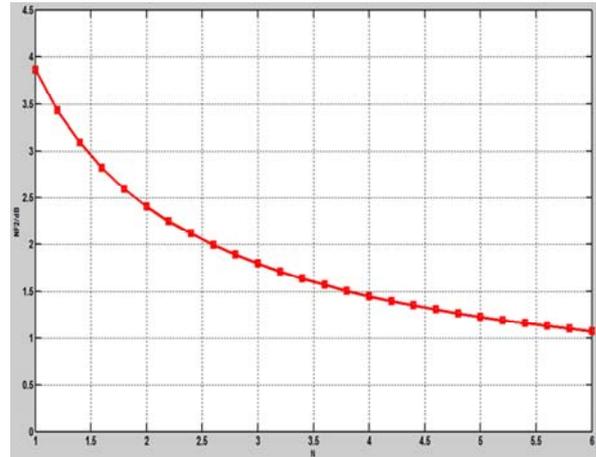

Fig.3 Noise figure NF2 of the CG–CS Topology for the Transconductance $g_{m,CG}$ is 20mS, R_S is 50Ω, γ is about 4/3, and the Load Resistors R_{CG} is about 1000Ω

With impeding matching of CG transistor M3, the noise figure can't be able to be reduced further. However, based on the inductively degenerated stage, the proposed balun-LNA achieves lower noise figure for the large R_S and small $g_{m,CG}$.

According to the noise figure cascaded formula, the total noise figure of the balun-LNA can be expressed as [11],

$$NF = NF1 + \frac{NF2 - 1}{A_{V,1}} \qquad (8)$$

Usually, the inductively degenerated cascade configuration has high voltage gain $A_{V,1}$. Therefore, NF1 has an important effect on the total noise figure NF of LNA.

D.   Gain and Phase Balance

The balun-LNA can provide the differential output signal, which is better suit for the following signal processing. Therefore, it is of great importance to make sure gain and phase balance of the CG–CS topology [13].
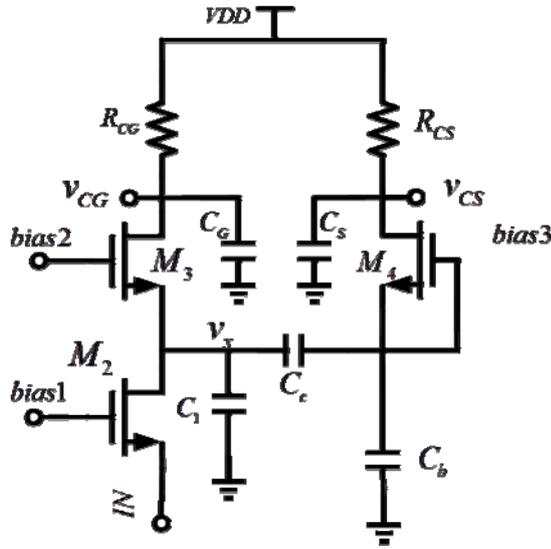
15.3

Fig.4 Schematic of the CG–CS Topology LNA

The schematic of the CG–CS topology with the parasitic effect is shown (Fig. 4), capacitor C1 is the total capacitor from M2, M3 and M4 and capacitor CG and CS is output capacitor [19]. The value of capacitor C1 is written as

$$C1 \approx C_{gd2} + C_{db2} + C_{gb4}(1 + g_{m,CS} \square R_{CS}) + C_{gs4} + C_{sb3} + C_{gs3}(1 + g_{m,CS} \square R_{CS}) \quad (9)$$

The voltage gain of CG-transistor can be expressed as

$$\frac{v_{CG}}{v_x} = \frac{g_{m,CG} \square R_{CG}}{1 + sR_{CG} \square C_G} \square \frac{1 + g_{m,CS} \square R_{CS} + sR_{CS} \square C_S}{1 + sR_{CS} \square C_S} \quad (10)$$

The voltage gain of CS-transistor can be expressed as

$$\frac{v_{CS}}{v_x} = -\frac{g_{m,CS} \square R_{CS}}{1 + sR_{CS} \square C_S} \quad (11)$$

Operating at the low frequency, gain and phase balance of the CG–CS topology can be easily achieved [13, 20, 21]. Considering the signal transmission from v_x to v_{CG} and v_{CS}, the imbalance of the gain and phase can be calculated as

$$\Delta\phi = \phi_{CS} - \phi_{CG} - 180$$
$$= \tan^{-1}(w \square R_{CG} \square C_G) - \tan^{-1}\left(w \square R_{CS} \square C_S / (1 + g_{m,CS} \square R_{CS})\right) \quad (12)$$

$$\Delta v = 20 \log_{10}(v_{CS}) - 20 \log_{10}(v_{CG})$$
$$= 20 \log_{10}\left(\sqrt{\frac{1 + (w \square R_{CG} \square C_G)^2}{1 + \left(w \square R_{CS} \square C_S / (1 + g_{m,CS} \square R_{CS})\right)^2}}\right) \quad (13)$$

From (12) and (13), the reducing ratio n ($n = g_{m,CS} / g_{m,CG}$) can further cancel the imbalance of the gain and phase. However, balance of the gain and phase would be affected for the high frequency fields.

F. Noise Canceling and Distortion

Considering the gain and phase balance, output signal of CG-transistor and CS-transistor should meet the equal gain and opposite phase [14]. And the output anti-phase voltage

noise of CG-transistor can be calculated as

$$v_{noise,CG} = -i_{in} \square R_{CG} \quad (14)$$

Where i_{in} is the input current noise, R_{CG} is the output resistor of CG-transistor. The output voltage noise $v_{noise,CS}$ of CS-transistor is the same as $v_{noise,CG}$ of CG-transistor, thus: $v_{noise,CS} = -i_{in} \cdot R_{CS} = v_{noise,CG}$. Therefore, the noise from the CG-transistor can be canceled.

With the nonlinearity of transistors, a controlled current source is modeled between drain and source. The output voltage difference of CG-transistor and CS-transistor can be written as,

$$\Delta v = v_{out,CG} - v_{out,CS} = v_{in} \square \frac{R_{CG}}{R_S} \quad (15)$$

Where v_{in} is the input information signal, RS is the source resistor. Linearity of CG-transistor can be determined by R_{CG}. From (14) and (15), the nonlinear noise and distortion of CG-transistor can be canceled. Therefore, the linearity of the CG–CS topology can be determined by the CS-transistor.

III. CIRCUITS DESIGN AND SYSTEM PERFORMANCE

The proposed balun-LNA is design in 65nm CMOS technology. In order to achieve the differential signal of equal amplitude and opposite phase, gain and phase balance of the CG–CS topology is considered with the noise and distortion canceling. Generally, the imbalance of the gain and phase is within *±0.5dB and ±5º* in the signal bandwidth of for most of IoT applications respectively. According to the above analysis, the ratio n between trans-conductance $g_{m,CS}$ and the trans-conductance $g_{m,CG}$ is 4, which can achieve the lower noise figure NF. In addition, the lower supply voltage of the MOS transistor can reduce the power consumption of LNA.

A. S-parameters of Balun-LNA

Based on the inductively degenerated structure, balun-LNA could be used to generate the differential output signal with the high gain and low noise figure. Operating at the 780MHz, input matching and output matching inductors and capacitors is very large so that the off-chip matching is adopted. The circuit simulation shows that the S11 of LNA is about -20dB and the voltage gain of LNA is about 30dB at the 780MHz shown (Fig. 5 (a)).
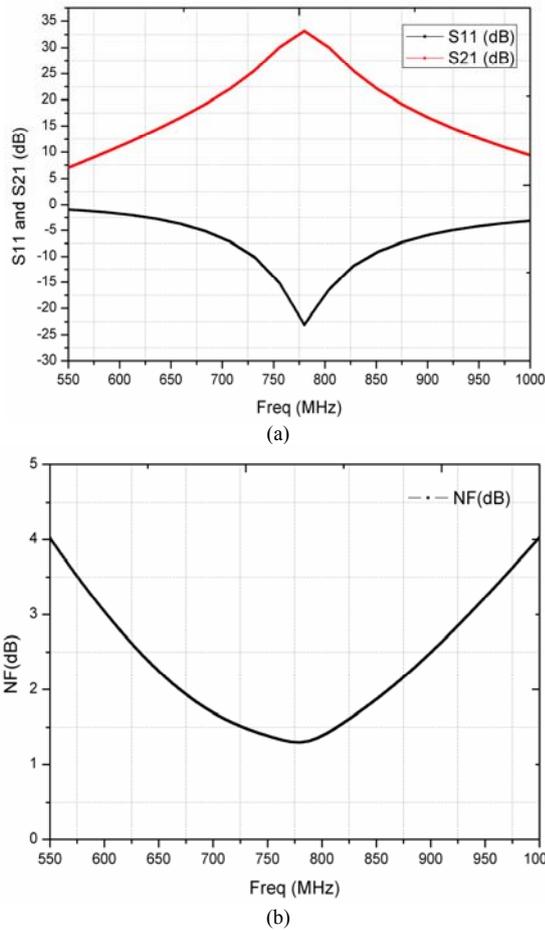
(a)

(b)
Fig.5 (a) S11, S21 of LNA, (b) NF of LNA

(a)

(b)
Fig.6 (a) S11, S21 of LNA, (b) NF of LNA(a) Gain Imbalance (b) Phase Imbalance of the CG–CS Topology

By using the inequality between trans-conductance gm,CS and the trans-conductance gm,CG , low noise figure can be achieved. The noise figure of the LNA spacing of 550MHz and 1GHz is shown (Fig. 5 (b)). The minimum NF is 1.5dB at the 780MHz.

B. Gain and Phase Imbalance

Further, the amplitude and phase imbalance of differential output signal remains within 0.5dB and 5 degrees in the signal bandwidth respectively as shown (Fig. 6 (a) and (b)). By adjusting to the bias of the CG–CS topology, gain and phase imbalance is reduced.
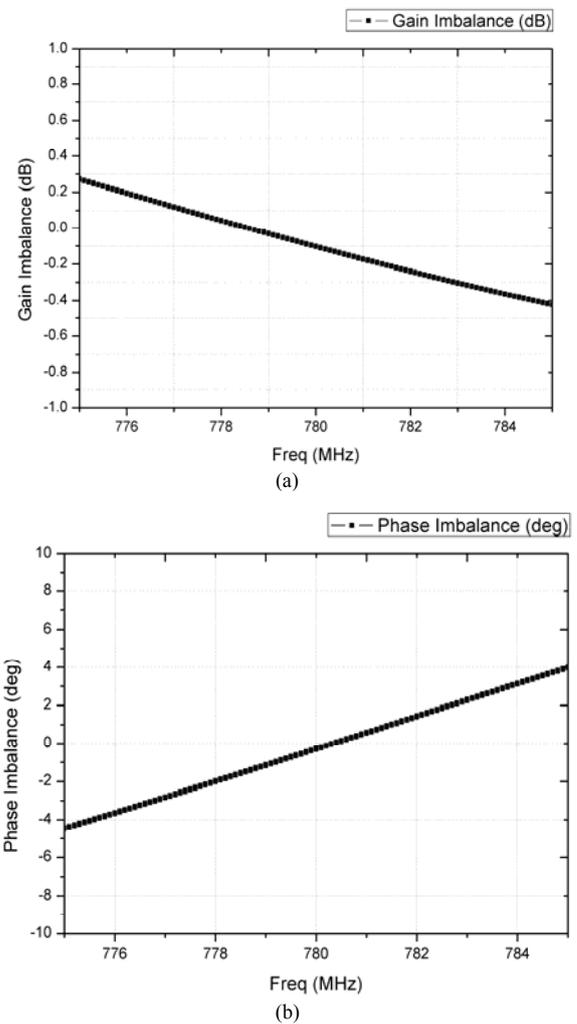
C. Performance

With the voltage supply of 1.2V, the current consumption of balun-LNA with noise-cancelling is 1.6mA.When the input RF frequency is 780MHz and input amplitude of signal is -90dBm. LNA can achieve better differential signal output at the data rate of 1Mbps. In addition, linearity of balun-LNA doesn't need to be considered for the subsampling architecture. Compared to others, the performance of the proposed LNA is listed in Table I. The proposed LNA has advantages than others in terms of noise figure and power consumption. Owing to the balun-LNA with the noise cancelling technique, noise figure can be improved. And the power consumption can be reduced by the controlling the bias of transistors.

TABLE I. ESTIMATED PERFORMANCE COMPARISON

	MWCL 11 [6]	TMTT 15 [7]	JSSC 08 [12]	TMTT 12 [13]	EL 10 [15]	This Work (simulation)
Technology(CMOS)	0.18um	0.13um	65nm	0.13um	0.18um	65nm
Frequency	900MHz	900MHz	0.2-.2GHz	0.2-2.0GHz	1.227GHz	780MHz
S11	--	-10dB	--dB	--dB	-14dB	-20dB
Noise figure	1.76dB	1.94dB	<3.5dB	3.8dB	1.8dB	1.5dB
Gain	15dB	18dB	13-15.6dB	7.6-16.6dB[b]	30.4dB	30dB
Power consumption	6.75mW (1.5V)	2.88mW （1.2V）	21mW[a] （1.2V）	3mW （1.2V）	3.6mW （1.8V）	1.92mW （1.2V）

[a] The total power consumption [b] Unloaded voltage gain of balun-LNA core

IV. CONCLUSIONS

The proposed balun-LNA for the subsampling architecture of receiver is analyzed in detail. The inductively degenerated cascade differential configuration achieves better matching, high gain and low noise figure. The inequality of trans-conductance $g_{m,CS}$ and the trans-conductance $g_{m,CG}$ provide lower noise figure. With noise canceling and distortion canceling, gain and phase balance of differential output signal are improved. The results show that the proposed balun-LNA has advantages in terms of noise figure and power consumption. Otherwise, linearity would be improved by highly linear-enhancement technique. Further, the advanced CMOS technologies reduce power dramatically and noise figure would be improved by Q-enhancement technique.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflicts of interest.

ACKNOWLEDGMENT

REFERENCES

[1] Zhicheng Lin, Pui-In Mak, Rui Martins, "A Sub-GHz Multi-ISM-Band ZigBee Receiver Using Function-Reuse and Gain-Boosted N-Path Techniques for IoT Applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2990-3004, Dec. 2014.

[2] Jakonis, Darius, et al, "A 2.4-GHz RF sampling receiver front-end in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1265-1277(2005).

[3] Meng, Fanzhen, et al, "A 780-MHz low power transceiver for wireless nodes applications in Internet of Things," *in Proc. IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS'13),* Columbus, Ohio, USA, Aug. 2013, 598 – 601.

[4] DeVries, Christopher, and Ralph D. Mason. "Subsampling architecture for low power receivers." *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 4, pp. 304-308, April 2008.

[5] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[6] T. H. Jin and T. W. Kim, "A 6.75 mW 12.45 dBm IIP3 1.76 dB NF 0.9 GHz CMOS LNA employing multiple gated transistors with bulk-bias control," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 11, pp. 616–618, Nov. 2011.

[7] Hong Gul Han, Doo Hwan Jung, and Tae Wook Kim, "A 2.88 mW 9.06 dBm IIP3 Common-Gate LNA With Dual Cross-Coupled Capacitive Feedback." *IEEE Transactions on Microwave Theory and Techniques,* vol. 63, no.3, pp. 1019-1025, Mar 2015.

[8] Xiaohua Fan, Heng Zhang, Edgar Sánchez-Sinencio. "A Noise Reduction and Linearity Improvement Technique for a Differential Cascode LNA." *IEEE J. Solid-State Circuits,* vol. 43, no. 3, pp. 588-599, Mar. 2008.

[9] Jack Li and S. M. Rezaul Hasan, "Design and Performance Analysis of a 866-MHz Low-Power Optimized CMOS LNA for UHF RFID." *IEEE Transactions on Industrial Electronics,* vol. 60, no. 5, pp. 1840-1848, May 2013.

[10] T.K.Nguyen, C. H. Kim,G. J. Ihm,M.S.Yang, and S.G.Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Techn.,* vol. 52, no. 5, pp. 1433–1442, May 2004.

[11] Fei Chen, Wei Zhang, Woogeun Rhee, et al, "A 3.8-mW 3.5–4-GHz Regenerative FM-UWB Receiver With Enhanced Linearity by Utilizing a Wideband LNA and Dual Bandpass Filters." *IEEE Transactions on Microwave Theory and Techniques,* vol. 61, no. 9, pp. 3350-3359, Sep 2013.

[12] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "THE BLIXER a wideband balun-LNA–I/Q-mixer topology," *IEEE J. Solid-State Circuits,* vol. 43, no. 12, pp. 2706–2715, Dec. 2008.

[13] Jusung Kim, Jose Silva-Martinez. "Wideband Inductorless Balun-LNA Employing Feedback for Low-Power Low-Voltage Applications." *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no.9, pp. 2833-2842, Sep 2012.

[14] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.

[15] Y. Ji, et al, "1.8 dB NF 3.6 mW CMOS active balun low noise amplifier for GPS," *IEEE Electronics Letters 4th,* vol. 46, No. 3, Feb. 2010.

[16] Yeo Myung Kim, Honggul Han, and Tae Wook Kim, "A 0.6-V +4 dBm IIP3 LC Folded Cascode CMOS LNA With gm Linearization." *IEEE Transactions on Circuits and Systems—II: Express Briefs*, vol. 60, no. 3, pp. 122–126, Mar 2013.

[17] Rafaella Fiorelli, Fernando Silveira, Eduardo Peral´ıas. "MOST Moderate–Weak-Inversion Region as the Optimum Design Zone for CMOS 2.4-GHz CS-LNAs." *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 3, pp. 556-566, Mar 2014.

[18] H. Samavati, H. R. Rategh, and T. H. Lee, "A 5-GHz CMOS wireless LAN receiver front-end," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 765–772, May 2000.

[19] H. T. Friis, "Noise figure of radio receivers," *Proc. IRE*, vol. 32, pp. 419–422, Jul. 1944.

[20] Behzad Razavi*, Design of Analog CMOS Integrated Circuits*. McGraw-Hill Education (Asia) Co. Press, 2001.

[21] M. A. Martins, P.-I. Mak, and R. P. Martins, "A single-to-differential LNA topology with robust output gain-phase balancing against balun imbalance," in *IEEE ISCAS*, May 2011, pp. 289–292.