Design of an Assembly Line Structure ADC

Chen Hu[1], Feng Xie[1],Ming Yin[1]

[1] *Department of Electronic Engineering*, Naval University of Engineering, Wuhan, China

***Abstract* — This paper presents a circuit design and simulation result for unit circuit and the overall circuit of assembly line structure ADC. Among the unit circuit, the sampling switch of sample holder uses a higher linearity bootstrapped switch, by using the bottom plate sampling to offset the effect of charge injection effect, and by using the capacitance flip type structure to reduce power consumption, designing a high gain and high speed operational trans-conductance amplifier to improve gain and speed. According to the influence of noise, the sampling capacitor is selected, and then the load operational amplifier is determined. Operational amplifier is the core module. Therefore it is very necessary to take design and simulation to it. the common mode level changes of MDAC input signal is smaller, we use the higher current efficiency sleeve type amplifier to save power consumption. In two-phase non overlapping clock circuit, a buffer is added to drive heavy load. Simulating the whole ADC circuit, we can get SNDR=72.3dB，SFDR=84.9dB, and the effective bit is 11.7.**

Keywords - ponent; assembly line ADC, MDAC, sample holder, bootstrapped switches

I. INTRODUCTION

With the technology development of very large scale integrated circuit, request of speed and accuracy of ADC (analog to digital converter) continuously improve. Assembly line ADC can provide excellent dynamic performance. This characteristic can satisfy ADC high speed, high accuracy requirements for the modern digital wireless communication system, high precision imaging system, and so on. This paper presents an assembly line structure ADC, who can provide excellent dynamic performance, and its effective bit can get 11.7.

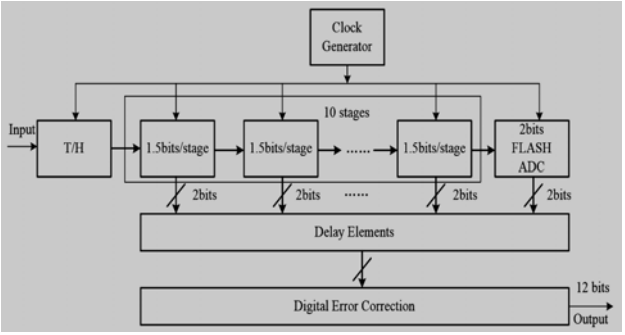

Fig.1 The overall block diagram of the ADC

II. DESIGN OF 1.5 BIT / STAGE MODULE CIRCUIT

The input of MDAC (Multiplying Digital to Analog Converter) is the first level output. Because of its small signal amplitude changes, the sampling switch must not use complex bootstrapped switch. Here we use the complementary switch. In addition, because the common mode level changes of MDAC input signal is smaller, we can use the higher current efficiency sleeve type amplifier to save power consumption. Below we will give a specific circuit design and simulation results.

A. Design of telescopic operational amplifier

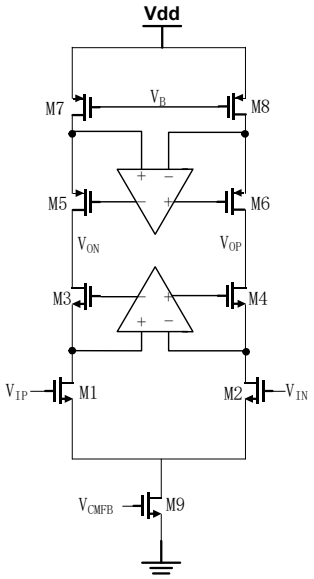

Fig.2 Telescopic cascade gain boosted operational amplifier

Figure2 shows the circuit diagram of telescopic operational amplifier. In order to improve the gain of the amplifier gain, the amplifier still uses the bootstrap structure. Compared with the folded operational amplifier, telescopic operational amplifier has only two current branches, so the telescopic operational amplifier is small in power consumption. In addition, because its second pole parasitic capacitance is relatively small, it has better high frequency characteristic. But the telescopic operational amplifier is composed of 5 layers of MOS tube superposition, so the input and output swing are reduced. This is the disadvantage of telescopic operational amplifier.

The method of determining parameters of the DC gain and the unity gain bandwidth product of telescopic operational amplifier is similar to the method of determining

parameters of the operational amplifier in sampling and holding device. The design principle and method of auxiliary operational amplifier with common mode feedback circuit are similar, so we don't detail here. According to the design index we can determine the width to length ratio of each MOS tube, and then we make open-loop AC simulation on telescopic operational amplifier firstly. The simulation result is shown in Figure 3. From the simulation results, we can see that the unity gain bandwidth product of the operational amplifier is 1.11GHz, and the DC gain is 101dB, and phase margin is 69 degrees.

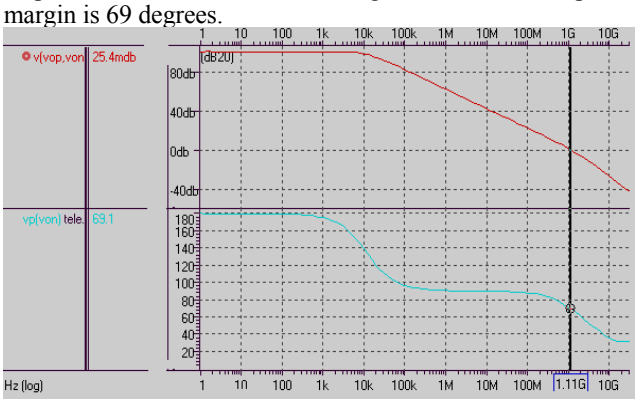

Fig.3 scopic casThe simulation results of the frequency characteristics

Then we made loop simulation. The simulation circuit is shown in Figure4, and the simulation results are shown in Figure5. According to the simulation result we can see that the loop gain is reduced to 93dB, and the loop unit gain bandwidth product is 542MHz, and the phase margin is 77.8 degrees. Compared with open circuit, the unity gain bandwidth product and DC gain all dropped a lot. This is caused by the low feedback coefficient.

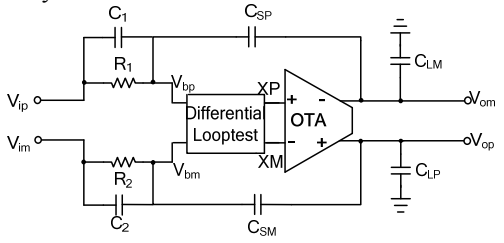

Fig.4 The loop simulation circuit in MDAC operational amplifier

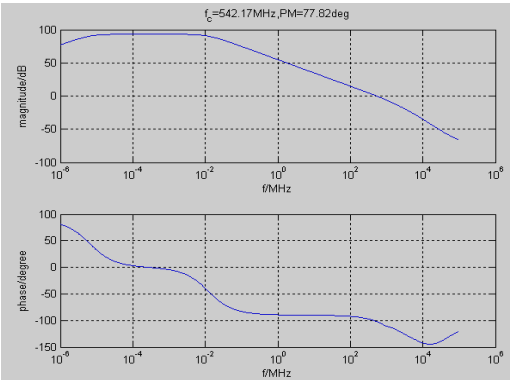

Fig .5 The simulation results of the loop frequency characteristic

Simulation result of the output swing characteristics of telescopic gain boosted operational amplifier is shown in Figure6. Through the simulation result, we can see that open loop DC gain is larger than 96.8dB, when the output difference is within -750mV~ +750mV.

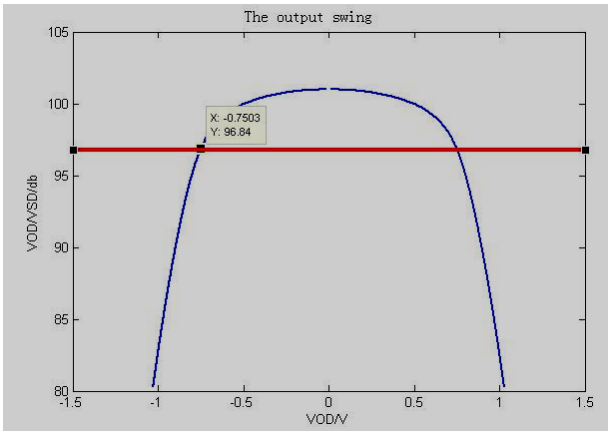

Fig.6 The output swing simulation results

B. *Design of sub ADC*

In 1.5 bit/ stage structure, each level output of 3 digital codes, therefore this structure require two comparators. After the output thermometer codes of the two comparator are encoded, we can obtain separately binary code and the digital code who can control sub DAC. Table I gives the relation between input and output of sub ADC.

TABLE I THE RELATION BETWEEN INPUT AND OUTPUT OF SUB ADC

V_{in}	D_1D_0
$-V_{ref}<V_{in}<-V_{ref}/4$	00
$-V_{ref}/4<V_{in}<+V_{ref}/4$	01
$+V_{ref}/4<V_{in}<+V_{ref}$	10

Figure.7 shows the circuit diagram of ADC. The comparator circuit introduced in front, so here will not go into. In Figure6, D1D0 respectively corresponding to MSB and LSB, DA~DC is used to control the signal of MDAC in DAC.

Adding a ramp signal on the input of sub ADC to make a test, we can get the simulation result as shown in Figure 8. In the figure, the first trellis show the input signal, and its change range is -750mV~+750mV. The second and third grids respectively correspond to D1, D0. From the simulation results, we can see that the voltage range of sub ADC is -184mV and 200mV. The theory of value is -187.5mV and +187.5mV, while the offset voltage of the digital correction circuit is 187.5mV. Therefore, the circuit can meet the design requirements.

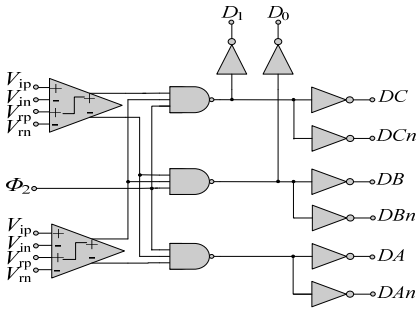

Fig .7 The circuit of sub ADC

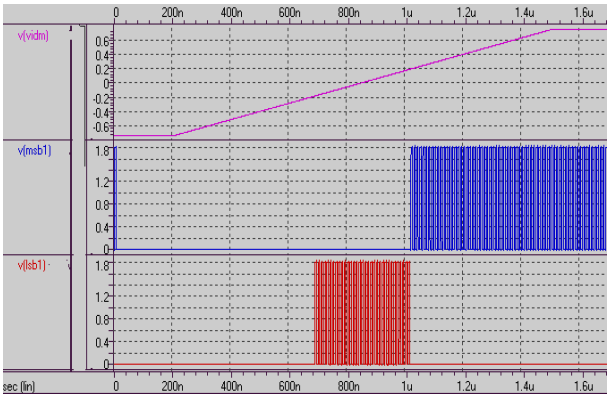

Fig. 8 The simulation result of sub ADC

The last stage is a parallel 2 bit ADC. The final level of post stage circuits on the circuit is not correct, so there is no redundancy. In fact, with the increasing series of requirements, the precision decreases gradually, especially the last grade need very low accuracy. So there is no need to correct. Table II gives the input and output diagram of FLASH ADC.

TABLE II THE RELATIONSHIP BETWEEN INPUT AND OUTPUT OF FLASH ADC

V_{in}	D_1D_0
$-V_{ref}<V_{in}<-V_{ref}/2$	00
$-V_{ref}/2<V_{in}<0$	01
$0<V_{in}<+V_{ref}/2$	10
$+V_{ref}/2<V_{in}<+V_{ref}$	11

The circuit structure of the FLASH ADC is shown in Figure9. D1, D0 respectively correspond to MSB and LSB. Simulating to the simulation the sub ADC, Adding a ramp signal on the input of sub ADC to make a test, the simulation result is obtained as shown in Figure10. From the results of simulation we can see the transformation voltage is -369mV、4mv、381mV, while the theory value is -375mV，0mV，+375mV. Disorder is far less than the final level of LSB. Therefore, the circuit can meet the design requirements.

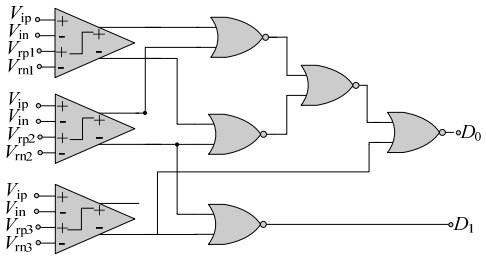

Fig. 9 The circuit of FLASH ADC

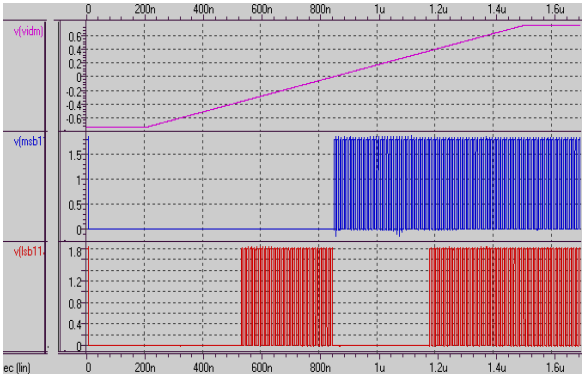

Fig .10 The simulation result of FLASH ADC

C. *Design of MDAC circuit*

After using switched capacitor feedback technology, the feedback capacitor is uncertain. Capacitor selection depends on the size of the input value. When the input value is between -1/4VREF and +1/4VREF, taking Cs as the feedback capacitance capacitor. When other values, taking Cs as the feedback capacitance capacitor. From table I and figure 4, we can get capacitor connection as shown in table III. From the table III we can see, when the -VREF<Vin<-1/4VREF or +1/4VREF<Vin<+VREF, Using Cs as the feedback capacitor, and at this point, Cf is connected to a fixed level. When the -1/4VREF<Vin<+1/4VREF, Using Cf as the feedback capacitor, and at this point, Cs is connected to a fixed level. Then we can get the circuit in Figure 11. In the figure, the symbolic in brackets are the representation of the signals that control the switch. When the DC is high, the corresponding switch K9 is closed. When the diameter of 2 DB and at the same time is in high level, the switch K10 is closed.

TABLE III THE CONNECTION AND INPUT RELATIONSHIP OF THE CAPACITANCE

V_{in}	Output	C_s	C_f
$-V_{REF}<V_{in}<-1/4\ V_{REF}$	00(DA)	FB	$-V_{REF}$
$-1/4V_{REF}<V_{in}<+1/4V_{REF}$F	01(DB)	GND	FB
$+1/4V_{REF}<V_{in}<+V_{REF}$	10(DC)	FB	$+V_{REF}$

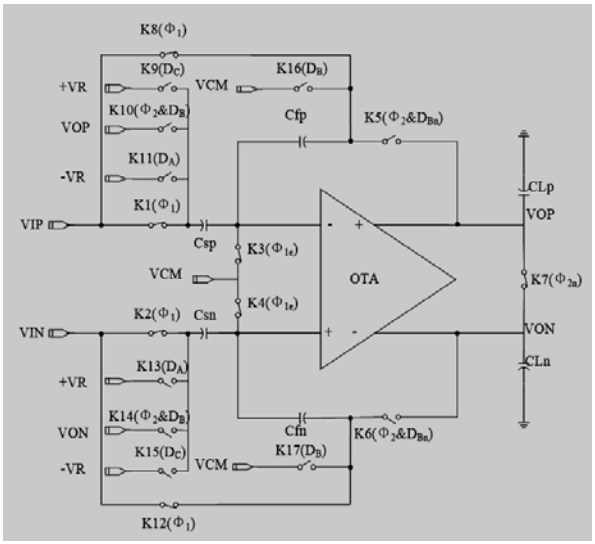

Fig .11 The MDAC circuit using switching capacitive feedback technology

III. DESIGN OF CLOCK GENERATION CIRCUIT D

Assembly line analog-to-digital converter is controlled by a two-phase non overlapping clock. And in order to overcome the charge injection effect, turning off clock early is needed. In addition, the control latch clock circuit is also needed. Two-phase non overlapping clock can be formed by mutual coupling NAND gate or NOR gate. When analyzing clock generating circuit, the steady state analysis should be performed firstly, then the transient analysis. Steady state analysis is to find out the steady state of input and output circuit of mutual coupled gate. For example, if coupled circuit is a NAND gate, when the two input NAND gate are respectively 0, 0, 1, 1, the circuit is stable. Transient analysis means corresponding changes in the output of the analysis when the input signals change. For example, when the phase of input clock changes, NAND gate input variable is 1, 0, 0, 1, and this state is a non steady state. If the initial input of the NAND gate is 1, 1, the output will response firstly, and the value changes from 0 to 1. This change leads to the input of another NAND gate into 1, 1, and the corresponding output is 0. While the input of the two NAND gate respectively 1, 1, 0, 0. The circuit reaches a steady state again.

Two-phase non overlapping clock circuit is shown in Figure12. In order to drive heavy load, buffer is needed here.

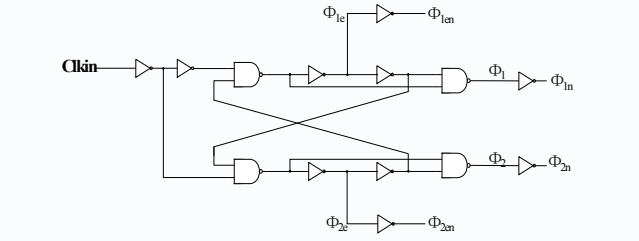

Fig.12 Two-phase non overlapping clock circuit

IV. DESIGN OF SAMPLING HOLDER

Sampling holder circuit is composed of analog switch, storage element and a buffer amplifier. It is located in front of the analog to digital converter. Comparing with the post stage circuit, the input signal changes are much larger in the amplitude and frequency. So the linear sample and hold circuit level is high. In order to improve the linearity of the sample holder and meet the requirements of high precision, this paper describes the design of a sampling holder.

A. The design of bootstrapped switch

Poor linearity of ordinary switch is not suitable for large signal and high precision application. The bootstrapped switch is often used in the high precision analog-to-digital conversion. Figure13 shows the circuit structure of the classical bootstrapped switch.

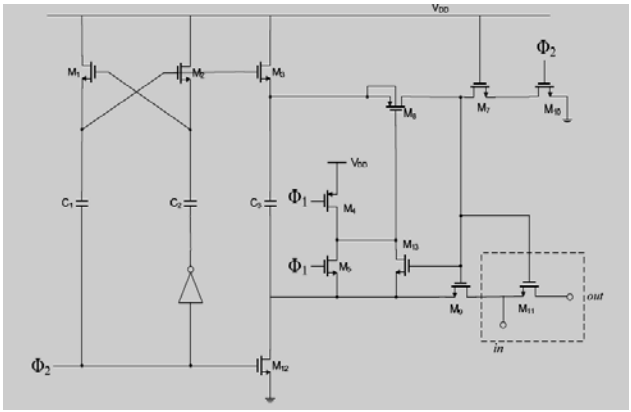

Fig.13 The structure of bootstrapped switch

In figure13, the M11 is the core of the switch For the transmission of the input signal, All the rest are auxiliary switch. Φ 1 and Φ 2 is a two-phase non-overlapping clock. M3 and M12 and capacitor C3 form a charging circuit. They will charge C3 to voltage on VDD. This makes the gate - source voltage of M11 to maintain in this constant value at turn-on state. The role of the cross coupling M1, M2 and C1, C2 on the left is to constitute a voltage multiplier circuit, and improve s the voltage of the gate terminal of M3 to make C3 fully charged. The role of M8 and M9 is to partition and conducting the loop made by C3 in M11 pipe gate source end. The M4, M5 and M10 control them through. M7 and M13 according to the M10 and M8 play a protective role. The value of C3 must be large enough to avoid charge leaked M11 gate end parasitic capacitance.

Figure14 shows the simulation results. The first line of the waveform is sine input signal and output signal. It can be seen that the output accurately track live input. Second waveform is the voltage differential between sampling switch gate terminal and the input terminal. The values in the conduction stage maintain a constant value to meet the purpose to increase the switch linearity.

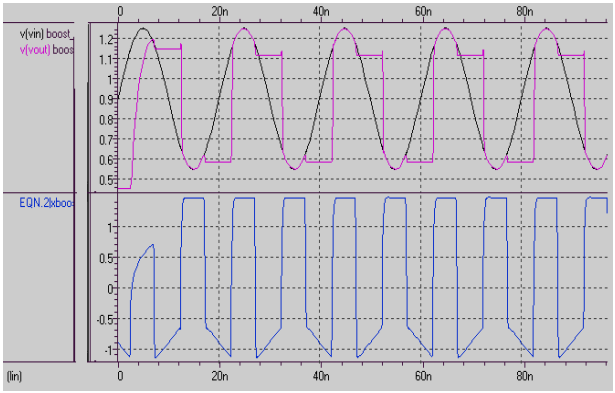

Fig.14 The bootstrapped switch waveform simulation

D. The select of the sampling capacitor

The sampling capacitor is selected according to the requirement of noise and signal to noise ratio. The sampling holder noise is mainly composed of sampling phase switch thermal noise and keep stage operational amplifier thermal noise. By the derivation of estimation, we can the output equivalent noise of sampling holder.

$$P_{n,TH} = \sigma_{n,track}^2 + \sigma_{n,hold}^2 = 2\frac{1}{\beta}\frac{k_B T_r}{C_s} + 2\frac{4}{3}\frac{1}{\beta}\frac{k_B T_r}{C_{Leff}} \quad (1)$$

SNR of analog-to-digital converter is:

$$SNDR = \frac{P_{sig}}{P_q + P_n} = 74dB \quad (2)$$

In the formula, Psig is the signal power, and Pq is quantization noise power, and Pn is the total noise power. Setting up quantization noise power and total noise power are equal, it can estimate the size of the sampling capacitor.

E. The design of operational amplifier

Operational amplifier is the key module in sampling holder. In order to realize the sampling holder with high speed and high precision, we need to design the operational amplifier with high DC gain, high bandwidth, and high swing. When designing, we should estimate operational amplifier index according to the sampling holder index to select the structure of the operational amplifier. Then we can choose parameters of each MOS according to the index value of amplifier, and adjust through simulation result. Because the circuit is fully differential structure, the design of the common mode feedback circuit is essential.

V. THE SIMULATION OF THE WHOLE CIRCUIT

Connecting sample holder and 1.5 bit / stage circuit, then simulate the whole ADC circuit. Setting the input signal peak to peak value to be 1.5V, frequency to be 49.609375MHz, and the sampling frequency to be 100MHz, then us take 256 point FFT analysis to sampling value. We get the spectrum in Figure15. According to the simulation result, we can get SNDR=72.3dB， SFDR=84.9dB, and the effective bit is 11.7. Table IV shows the comparison of design indexes and the pre-simulation results.

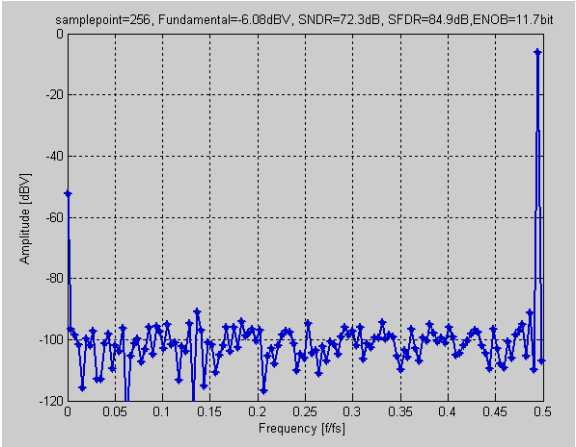

Fig.15 The dynamic simulation results of ADC

TABLE IV THE COMPARISON OF DESIGN INDEXES AND THE PRE-SIMULATION RESULTS OF THE ADC

	design indexes	Pre-simulation
supply voltage (V)	1.8	1.8
peak-to-peak of input(Vpp)	1.5	1.5
The frequency of input signal (MHz)	49	49
sampling frequency (MHz)	100	100
NSR (dB)	>68	72.3
Effective bits (bits)	>11	11.7
No stray dynamic range (dB)	>78	84.9

VI. CONCLUSION

This work presents a circuit design and simulation result for unit circuit and the overall circuit of assembly line structure ADC. According to the influence of noise, the sampling capacitor is selected, and then the load operational amplifier is determined. Operational amplifier is the core module, therefore it is very necessary to take design and simulation to it. the common mode level changes of MDAC input signal is smaller, we use the higher current efficiency sleeve type amplifier to save power consumption. In two-phase non overlapping clock circuit, a buffer is added to drive heavy load. The next step we plan to adopt double sampling technique. Double sampling technology shares operational amplifiers, so it increases complexity and design difficulty, but the rate can be exponentially improved.

ACKNOWLEDGMENT

This work was partially supported by National Defense Pre-research Foundation 9140A27020314JB11438.

REFERENCES

[1] Choksi O. & L. R. Carley. Analysis of Switched-Capacitor Common Mode Feedback Circuit . IEEE Transactions on Circuits and Systems. vol.50, No.12,pp. 906-917. 2003.

[2] Arias J. & V. Boccuzzi. Low-power pipeline ADC for wireless LANs [J]. IEEE Journal of Solid-State Circuits, vol.39, No. 08,pp. 1338-1340,2004.

[3] Lee B.G & B.M. Min. Opamp and capacitor sharing scheme for low power pipeline ADC[P] . US Patent, 2007.

[4] Bult K. & J.G. Geelen. A fast-settling CMOS op amp for SC circuits with 90-dB DC gain [J], IEEE Journal of Solid-State Circuits, vol.25, No. 06,pp1379-1384,1990.

[5] Kamath B.Y.T & R.G.. Meyer. Relationship between frequency response and settling time of operational amplifiers [J], IEEE Journal of Solid-State Circuits, vol.9, No. 06,pp. 347-352, 1974.

[6] Christopher Peter Hurrell, An 18 b 12.5 MS/s ADC with 93 dB SNR [J], IEEE Journal ofSolid-State Circuits, vol.45, No. 12, pp. 2647-2654, 2010.

[7] Marcu, Cristian. A 90nm CMOS low-power 60GHz transceiver with integrated baseband circuitry, IEEE Journal of Solid-State Circuits, vol.44, No. 12, pp. 314-315, 2009.

[8] Yuh-Min Lin, Beomsup Kim, Paul R. Gray, A 13-b 2.5-MHz Self-Calibrated Pipelined A/Dconverter in 3-μm CMOS , IEEE Journal of Solid-State Circuits, vol.9, No. 06,pp. 628-636, 1991.

[9] H. S. Lee, D. A. Hodges, P. R. Gray. A Self-Calibrating 15 bit CMOS ADC converter [J]. IEEEJournal of Solid-State Circuits, vol.19, No. 06,pp. 813-819,1984.

[10] B Razavi, Design techniques for high-speed, high-resolution comparators [J], IEEE Journal of Solid-State Circuits., vol.17, No. 12,pp. 1916-1926,1992.

[11] Xu,Ruoyu. Digitally calibrated 768-kS/s 10-b minimum-sizeSARADCarray with dithering [J],IEEE Journal of Solid-State Circuits, vol.47, No. 09,pp. 2129-2140,2012.