FPGA Implementation of Region Growing-Global Inhibition Segmentation Algorithm

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Abstract — The image segmentation is an important foundation for machine mobile object recognition. With the constant development of machine vision application technology, all image segment methods are appeared. Meanwhile, machine vision application technology is developed towards the high-level integration. The paper has presented a region growing-overall suppressing segmentation algorithm. The main frame of image segmentation network structure is completely applicable to digital circuit and can realize the parallel processing of image pixel cell. Therefore, the computational logic structure is proposed for this algorithm and FPGA is implemented according to the logic structure to obtain simulation result. The simulation result shows the calculated FPGA implementation realizes the target of image segmentation. The parallel computation can be implemented among pixel cells. Compared with the traditional image segmentation algorithm, it can greatly reduce the computation time. The computation FPGA provides theoretical and technical preparations for future real-time image process and a new method for the implementation of machine mobile object recognition.

Keywords - image segmentation; integrated circuit; Region Growing-Global Inhibition Segmentation Algorithm (RG-GISA).

I. FOREWIRD

The image segmentation is an important foundation for machine mobile object recognition. With the constant development of machine vision application technology, all image segment methods are appeared [1]~[5]. Meanwhile, machine vision application technology is developed towards the high-level integration [6]~[8].

The present image target tracking algorithm can be roughly divided into the following three kinds: time-based segmentation algorithm, space-based segmentation algorithm and segment algorithm in combination with time and space. Now we will give a brief introduction to the three algorithms [11]~[15].

The time-based segment algorithm is to recognize the target through simple algorithm. The most popular algorithm is background difference and inter-frame difference method. The background different method is an algorithm that detects the image target by comparing the current background reference model of image sequence. This algorithm is very practical and efficient. However, it is sensitive to the complex environment, environmental disturbance and noise. The adjacent inter-frame difference method is a detection method that contrasts and calculates the difference of adjacent two frame video images to recognize the mobile object target. This algorithm has strong adaptability to environment. However, it cannot detect the complete target but obtain some information of mobile target. It is not sensitive to the object mobile slowly. Thus, it has some limitations. The segmentation algorithm in combination with time and space divides the video image into combined regions through time and space-based boundary information and combines regions with similar mobile information. However, the edge detection and calculation of edge motion parameters are too complex. The space-based segment algorithm can be further divided into four kinds, including pixel classification method, edge detection method, regional segmentation method and model method. The pixel classification is easy to recognize the noise point or isolated point as an object. The threshold for classification largely depends on image contrast ratio. The edge detection method-based region recognition can be divided into two steps, including edge detection and labeling edge surrounded region. In addition, edge detection is very sensitive to noise point. The region segmentation is right for extraction of corresponding region.

LEGION is a region segmentation algorithm based on network element and describes the relation between network cells. The network cell-based algorithm has high parallel computing power. Therefore, it is very applicable to hardware-based algorithm implementation. The advantages are as follows: (a) it has high robustness for noise; (b) region segmentation can be finished in short time; (c) the image pixel can conduct parallel processing completely.

The paper uses FPGA to realize good timeliness and high level integration [9]~[10]. The paper researches FPGA implementation technology of Region Growing–Global Inhibition Segmentation Algorithm, RG-GISA and designs to implement FPGA implementation system of Region Growing–Global Inhibition Segmentation Algorithm.

II. INTRODUCTION OF RG-GISA ALGORITHM

(1) Model analysis of RG-GISA algorithm

The network of LEGION algorithm is composed by relaxation oscillators as basic unit. Fig. 1 shows a two-dimensional network structure connected simply and locally. Each oscillator except the boundary is just connected with its own adjacent regions to compose an oscillation network. In addition, an overall suppressor is included. The overall suppressor receives all oscillator activations from two-dimensional network and feeds back to each oscillator.

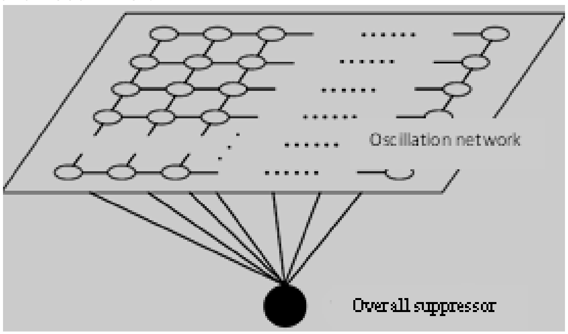

Fig.1 Two-dimensional Oscillation Network Structure

From Fig.(1), it can be seen that two-dimensional oscillation network consists of simple relaxation oscillators and is defined as the feedback loop between excitement factor x_i and inhibition factor y_i, It is expressed as:

$$dx_i/dt = 3x_i - x_i^3 + 2 - y_i + \rho + I_i H(p_i + \exp(-\alpha t) - \theta) + S_i \quad (1)$$

$$dy_i/dt = \varepsilon[\gamma(1+\tanh(x_i/\beta)) - y_i] \quad (2)$$

Formula (1) introduces a step function paraded H(v) under the basic structural model of oscillator. It can draw a conclusion that an oscillator of p_i being larger than θ refers to oscillation leader.

The variable p_i is defined as side potential of oscillator. The side potential is intruded to better segment images and inhibit noise region.

The definition formula of side potential is:

$$\dot{p}_i = \lambda(1-p_i)H\Big(\sum_{k\in N_1(i)} T_{ik} H(x_k, \theta_x) - \theta_p\Big) - \mu p_i \quad (3)$$

T_{ik} in Formula (3) refers to the fixed link weight defining network topology, $\lambda>0$. $N_1(i)$ refers to side potential in the adjacent region of oscillator *i.* If the activation in each adjacent region is larger than the threshold θ_x, the fixed link weight T_{ik} will be accumulated. If the accumulation is larger than θ_p, the value of step function paraded becomes 1. Meanwhile, the oscillator *I* will become an oscillation leader.

In order to produce high side potential, these regions shall exceed the threshold θ_x during the oscillation process.

The definition of coupling term S_i is:

$$S_i = \sum_{k\in N_2(i)} W_{ik} H(x_k - \theta_x) - W_Z H(z - \theta_Z) \quad (4)$$

Formula (4) includes the activation from the adjacent regions of oscillator *I* and the inhibition from overall suppressor. Where, W_{ik} refers to link weight between oscillators *k and i* and $N_2(i)$ refers to the collection of another adjacent region connecting with oscillator *i*. It is called as coupling region. W_z is the suppressed weight of overall suppressor *z*.

It can be seen that two adjacent regions are introduced in the algorithm, $N_1(i)$ and $N_2(i)$. $N_1(i)$ decides whether oscillator is the leader of local oscillation and $N_2(i)$ decides which oscillators can affect *I* activation. Generally speaking, the larger $N_1(i)$ is, the better it is.

In order to promote synchronization and non-synchronization, let's suppose that two synaptic weights are appeared between two oscillators. The fixed link weight T_{ik} refers to the fixed structure of oscillation network. The dynamic link weight W_{ik} can be changed rapidly with the time. W_{ik} is generated according to T_{ik} and dynamic normalization mechanism. The dynamic standardization is implemented by the differential equation, as shown in the following formula:

$$\dot{u}_i = \eta(1-u_i)I_i - \nu u_i \quad (5)$$

$$\dot{W}_{ik} = W_T T_{ik} u_i u_k - W_{ik} \sum_{j\in N(i)} T_{ij} u_i u_j \quad (6)$$

The function u_i is to measure whether the oscillator i is activated and is initialized as 0. Parameter η decides the refresh rate of u_i function.

Assume that the initial value W_{ik} of is 0 for all oscillators i and k. it can be found that if oscillator i is not activated, W_{ik} for all k is still 0. If the oscillator k is not activated, $W_{ik} = 0$ for all oscillators i. If at least one $k \in N2(i)$ meet the conditions of $u_i = 1$, $u_k = 1$, and then:

$$W_{ik} = W_T T_{ik} u_i u_k \Big/ \sum_{j \in N(i)} T_{ij} u_i u_j$$

and

$$\sum_{k \in N(i)} W_{ik} = W_T$$

Thus, the total link weight is transferred into weight of single oscillator and is equal to W_T. It is standardized.

In Formula (4), W_Z refers to suppressed weight from the overall suppressor. The definition of overall suppressor is as shown below:

$$\dot{z} = \phi(\sigma_\infty - z) \tag{7}$$

If one oscillator in the oscillation network is at active state, and then all overall suppressors are activated. θz is a threshold. If the activation of each oscillator is less than the threshold θz, and then the overall suppressor will not receive any input. Under this condition of $z \rightarrow 0$, oscillator in oscillation network cannot be suppressed. However, if the activation of one oscillator exceeds the threshold, the overall suppressor will receive input. Under this condition, $z \rightarrow 1$, when z activation exceeds the threshold θz, all oscillators in the oscillation network will be suppressed by overall suppressor. ϕ parameter decides the suppressor's reaction extent to activation. It is generally a decimal less than 1.

When multi-connection objects are mapped into the network, the local connection organizes the each object oscillator. This grouping is generated in oscillator at synchronous state. The overall suppressor is to suppress oscillation of different objects.

(2) RG-GISA algorithm optimization and extraction

For a gray level image, each pixel point in the image corresponds with the oscillator of oscillation network in the algorithm model suggested in the previous section. Moreover, each oscillator must be assumed to be at activated state when the image applies the algorithm network. The maximum difference between a gray level image and binary image is how to set up the connection, for a gray level image, the coupling strength between two adjacent oscillators depends on similarity of two corresponding pixel points.

In order to segment a real image with lots of pixel, please integrate formulas (1-7). In order to avoid a large number of computations, an algorithm is extracted from formulas (1-7). This algorithm accords with main steps of differential equation numerical simulation and shows main features of relaxation oscillator.

The approximate treatment is made during the algorithm extraction process:

1) When no oscillator is at activated state, the oscillator of all oscillators that can be activated with nearest distance from the up-jumping point (LK, left knee) will jump into activated state.
2) If an oscillator can receive actions from oscillators and general oscillator in adjacent regions, it needs a time period to jump up and enter at activated state.
3) The activated state and silence state can be switched within one clock period.
4) If no oscillator can jump up, all oscillators at the activated state will jump down. Under this condition, all oscillators activated by the same pattern will jump back.

The approximate treatment of 1)- 4) can be made to extract the following algorithm:

Only x value of oscillator i is used in the algorithm. $N(i)$ is the eighth adjacent region after removing boundary pixel. LKx, RKx and LCx refer to three angles of zero curves. LK and RK refer to left and right inflection points and LC refers to top left corner of curve. In order to make the computation simple, please assume that $LKx = -1$, $LCx = -2$, $RKx = 1$. I_i refers to brightness of pixel point i and IM refers to the maximum possible brightness of all pixels.

A. Initialization

Set z(0) = 0;

Calculate the link weight of oscillator i:

$$W_{ij} = I_M / (1 + | I_i - I_k |), k \in N(i)$$

Seek oscillation leader:

$$p_i = H[\sum_{k \in N(i)} W_{ik} - \theta_p]$$

Generate a random sequence and give a random initial state of each oscillator of network to make them distributed between LC_x and LK_x.

B. Seek oscillator j meeting the following conditions:

a. $x_j(t) \geq x_k(t)$, oscillator k is located in LB (left branch);
b. $p_j = 1$;

If conditions are satisfied, and then:

$x_j(t+1) = RK_x$; $z(t+1) = 1$

$x_k(t+1) = x_k(t) + (LKx - x_j(t))$,

Where, $k \neq j$

The oscillation leader that is located in *LB* (left branch) and close to *LK* (left knee) is selected in this step. The oscillation leader jumps to *RB* (right branch) and other all oscillators approach to *LK* (left knee).

C. Cycle to the following steps until the end:

a. If ($x_i(t) = RK_x$ && $z(t) > z(t-1)$), and then $x_i(t+1) = x_i(t)$;

b. If ($x_i(t) = RK_x$ && $z(t) \leq z(t-1)$), and then $x_i(t) = LC_x$; $z(t+1) = z(t) - 1$, oscillator i jumps down; if $z(t+1) = 0$, please go to the second step;

c. If the oscillator is at LK_x, please calculate oscillator i coupling strength:

$$S_i(t+1) = \sum_{k \in N(i)} W_{ik} H(x_k(t) - LK_x) - W_z H(z(t) - 0.5)$$

If $S_i(t+1) > 0$, oscillator *i* jumps, or else remains unchanged.

Compare the above algorithm and formulas (1-7), it can be seen that the following simplification is made:

Firstly, the dynamic link weight W_{ij} is directly set as $W_{ij} = I_M / (1 + |I_i - I_k|)$, $k \in N(i)$ The reason is that if the brightness values of pixel points i and j are closer, the corresponding oscillator coupling is stronger. Meanwhile, synchronization can be easily achieved.

Secondly, the oscillation leader is selected during initiation and decided before several periods of oscillation. As each oscillator is activated and weight is set, it is easy to forecast which oscillators will become the leader to reduce the computation time.

The above extracted algorithm greatly simplifies formulas (1-7) and reduces the time of overall computation. Moreover, the corresponding steps are given for the specific implementation of algorithm.

III. LOGICAL STRUCTURE OF CALCULATING SYSTEM

The flow chart of segmentation algorithm can be obtained through RG-GISA algorithm. From the analysis of flow chart, it can be seen that this algorithm consists of three modules, link weight calculation module, oscillator leader judgment module and image segmentation network module, as shown in Fig. (2):

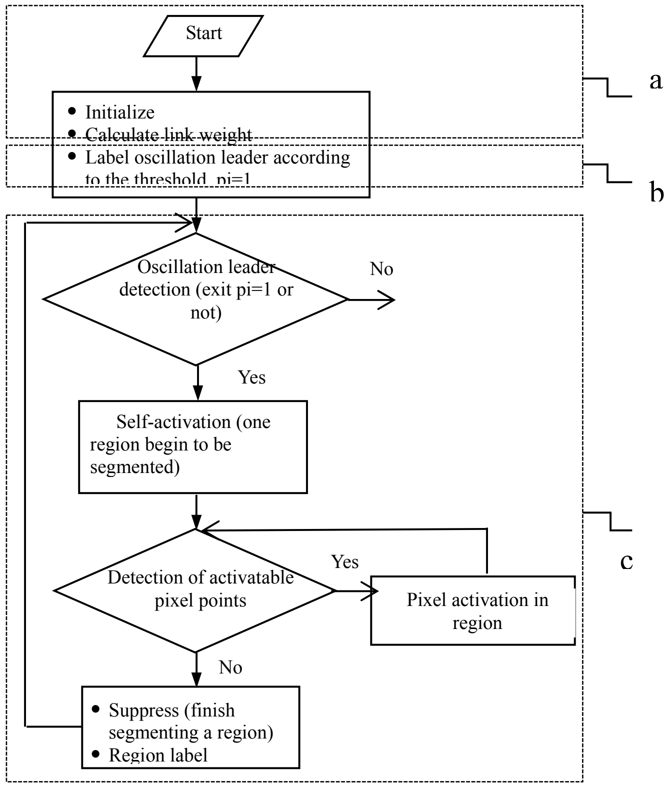

Fig.2 Module division of segmentation algorithm

Logic structure of overall calculating system designed according to RG-GISA calculation features, image input and segmented object feature sequence extraction can divide the image target recognition algorithm FPGA logic design into 5 modules, as shown in Fig. (3).

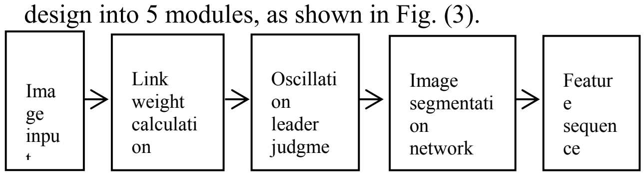

Fig.3 RG-GISA Logic Structure of Calculating System

A. Image segmentation network module design

The image segmentation module is a central module of segmentation algorithm. This module contains two parts. The first part is to seek the location of oscillation leader and the second part is to activate all activation points in the region through the oscillation leader, that is, segment the object in the location of oscillation leader.

The structural chart of image segmentation network module is shown in Fig. (4):

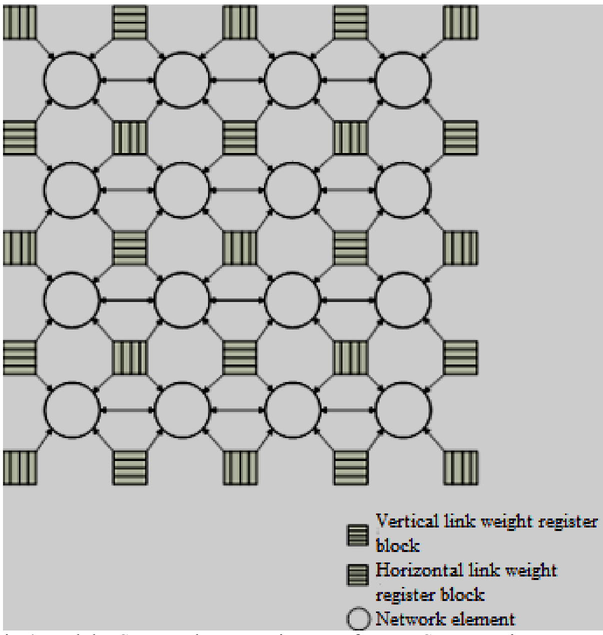

Fig.4 Modular Structural Frame Diagram of Image Segmentation Network

All network cells in image segmentation network in Fig.(4) are mutually connected. The network cell expresses three meanings here, including pixel point of image, oscillator of network and each inhibiting factor that makes up overall suppressor.

We adopt the method of oscillation leader leveling-passing. The oscillator leader just needs an overall scanning during the whole image segmentation with this method. The structural frame is shown in Fig. (5):

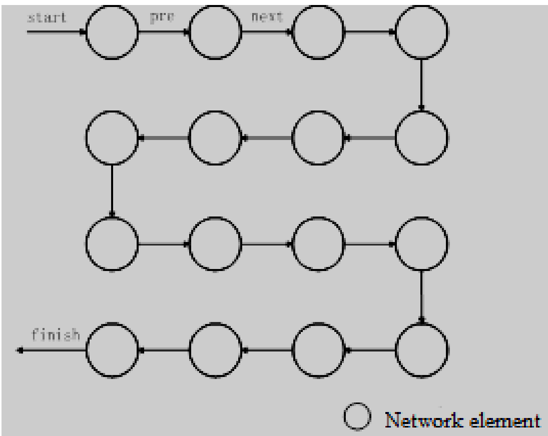

Fig.5 Structural Frame with LP Method

For the oscillation leader labeling-passing method, when pre_{ij} = 1, oscillator of network cell can be judged as the oscillation leader or not based on whether P_{ij} is equal to 1. If P_{ij} = 0, and then $next_{ij}$ = 1, n_{ij} = 0. Where, n_{ij} refers to labeling position of network cell. If P_{ij} = 1, and then nextij = 0, n_{ij} = 1, the location of oscillator leader is determined. Moreover, regional activation corresponding to oscillator leader begins to be implemented.

The activation of network cell in the segmentation network depends on the oscillator state in the eight adjacent regions of network work and link weight. If a network cell is at activated state, the link weight of two network cells is accumulated. When the accumulation exceeds the threshold of overall suppressor, the network cell is activated, or else, at non-activated state. The frame structure is shown in Fig. (6):

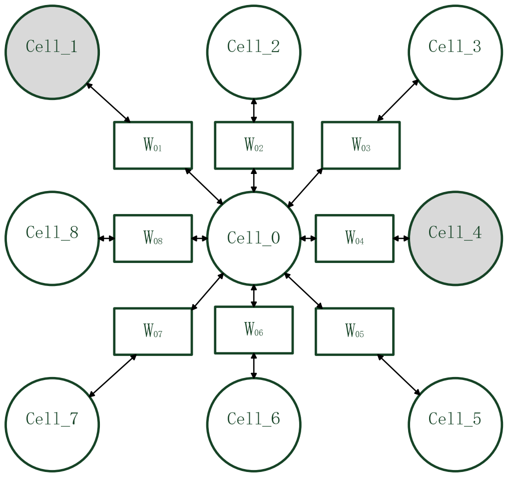

Fig. 6 Frame Structure Judged by Network Cell State Change

If you want to judge whether Cell 0 network cell in Fig. 5 is activated, firstly, you shall judge the state of Cell_1~Cell_8 of Cell_0. Cell_1 and Cell_4 network cells are at activated state. Therefore, if the accumulation is larger than the overall suppressor threshold, and then Cell_0 is activated, or else at non-activated state.

The inhibiting factor phase of network cell in the segmentation network decides whether the overall suppressor suppresses the network of segmentation network. If the phase or value is 0, the suppression can be fed back to all network units, or else it cannot have suppression function. The frame structure is shown as Fig.(7):

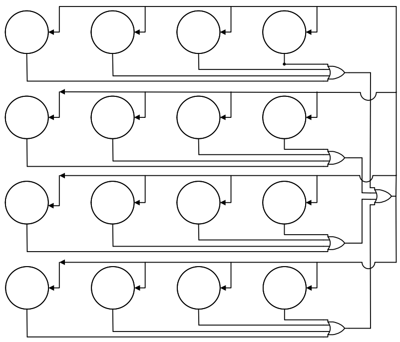

Fig.7 Overall Suppressor Inhibitory Factor and Feedback Frame Diagram

It can be seen from the design of image segmentation network module that the module is established on the link weight module and oscillation leader judgment module. The first two modules provide data support for segmentation network module.

B. Link weight calculation module

It can be seen from the structural frame of image segmentation network module that the link weight register can be divided into two kinds, vertical link weight register and horizontal link weight register. The vertical link weight calculation corresponds to even network cell in even number line and odd network cell in odd number line. The horizontal link weight calculation corresponds to odd network cell in even number line and even network cell in odd number line.

Each link weight module consists of 4 small modules. These 4 small modules separately show link weight of pixel cell, as shown in Fig.(8).

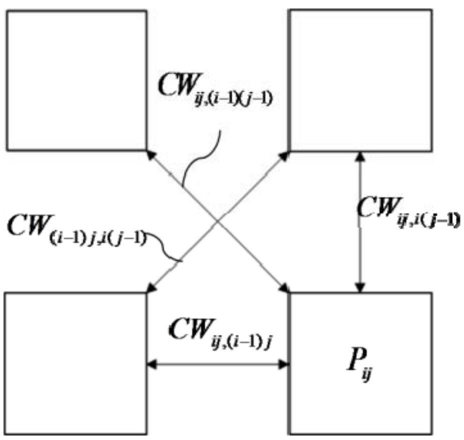

Fig.8 Link Weight Calculation Model

In addition, the calculation of link weight involves division operation, as shown as follows:

$$W_{ik} = I_{max} / (1 + |I_i - I_k|),\ k \in N(i) \qquad (8)$$

In order to avoid the division operation of Formula (8), it is analyzed that only the calculation of $|I_{ij} - I_{kl}|$ is made in FPGA implementation structure. The link weight is appeared in 3bits through 8bits-3bits encoder. The method can reduce the complexness of logic structure and storage space. The structure is shown in Fig. (9).

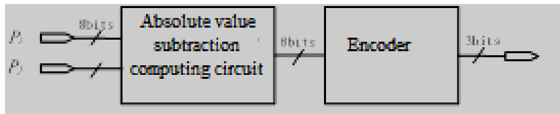

Fig.9 Link Weight Calculation Module Frame Structure

B. Oscillation leader judgment module

The sum of network cell and link weight of eight adjacent regions can decide whether the network cell is the oscillation leader. If the value is larger than the oscillation leader threshold, the network cell is the oscillation leader and is labeled as $P_i = 1$, or else, $P_i = 0$.

The frame structure of oscillation leader judgment module is shown in Fig. (10):

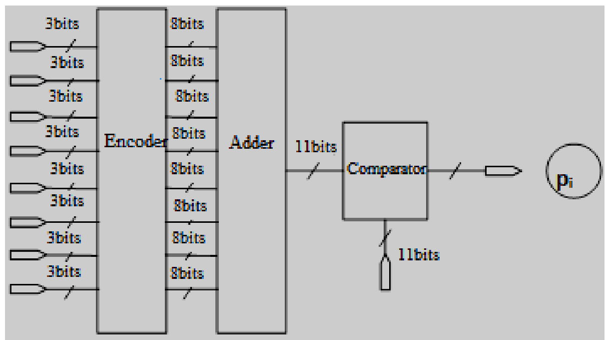

Fig.10 Oscillation Leader Judgment Module Frame Structure

IV. FPGA IMPLEMENTATION STRUCTURE AND SIMULATION RESULT

The paper segments a 10x10 image module, as shown in Fig. (11) below:

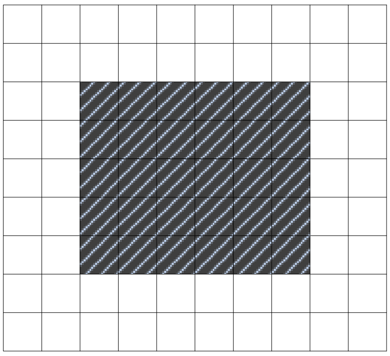

Fig.11 10x10 Image Module

A. FPGA implementation and result analysis of link weight computation module

The link weight computation module is a selector to read the image data information form ROM according to the sequence and sends the image information to another arranged selector. Moreover, it sorts the adjacent regions of link weight for each pixel cell according to rules. Later, it integrates eight adjacent regions of each pixel cell, calculates the link weight and finally stores them.

The simulation result is shown in Fig.(12):

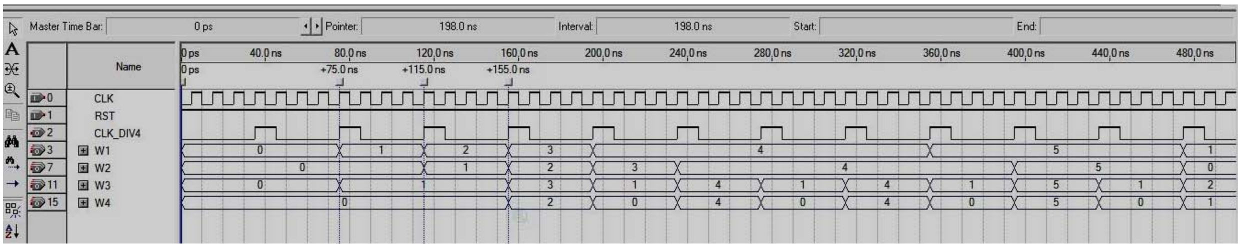

Fig. 12 Simulation Result of Link Weight Calculation Module

W1, W2, W3 and W4 are defined four-adjacent-region link weight. Ensure to store the calculated link weight.

C. Oscillation leader judgment module FPGA implementation and simulation result

The link weight calculation module provides required data support for oscillation leader judgment module. The comparison between the accumulation of pixel cell in eight adjacent regions and threshold can decide the location of oscillation leader and store the location. It provides the data support for image segmentation network module with the link weight together.

In order to improve the processing speed, FPGA hardware design advantage and parallel processing method are adopted, that is, it can process a list of pixels within each clock period. Thus, it only needs 10 clock periods to calculate the oscillation leader location of the whole network.

The simulation result of module is shown in Fig.(13)below:

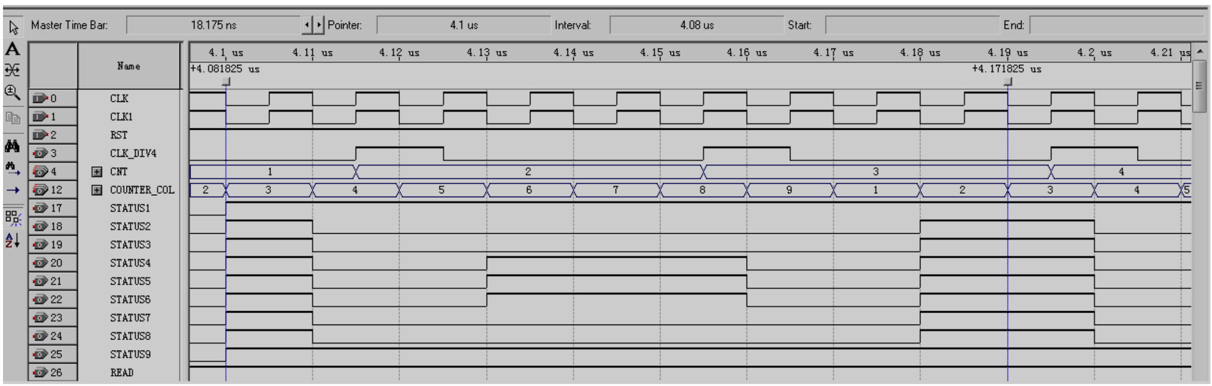

Fig. 13 Module Simulation Result Judged by Oscillator Leader

From the simulation result judged by oscillation leader, it can be see that the module finds out the location of oscillation leader from the image network, labels the oscillator leader unit as 1 and stores as the image segmentation network modular service.

D. Image segmentation network module FPGA implementation and simulation result analysis

The image segmentation network module is the key module for the algorithm. The link weight calculated by the first two modules and oscillator leader location serve for the module.
Each pixel cell is an independent network cell in this module, that is, all network cells are parallel structures. However, all network cells can interact with each other. Seek in serial when seeking the oscillation leader.
Ensure to segment 10x10 image module. The simulation result is shown in Fig.(14) below:
G_INHIBITOR in Figure refers to overall suppression value. It can be seen that the input image is segmented into two regions, Regions A and B. Xi_ROW0, Xi_ROW1, Xi_ROW2, Xi_ROW3, Xi_ROW4, Xi_ROW5, Xi_ROW6, Xi_ROW7 and Xi_ROW8 refer to growing status of each list of pixel cells. STARTPRE refers to starting clock.

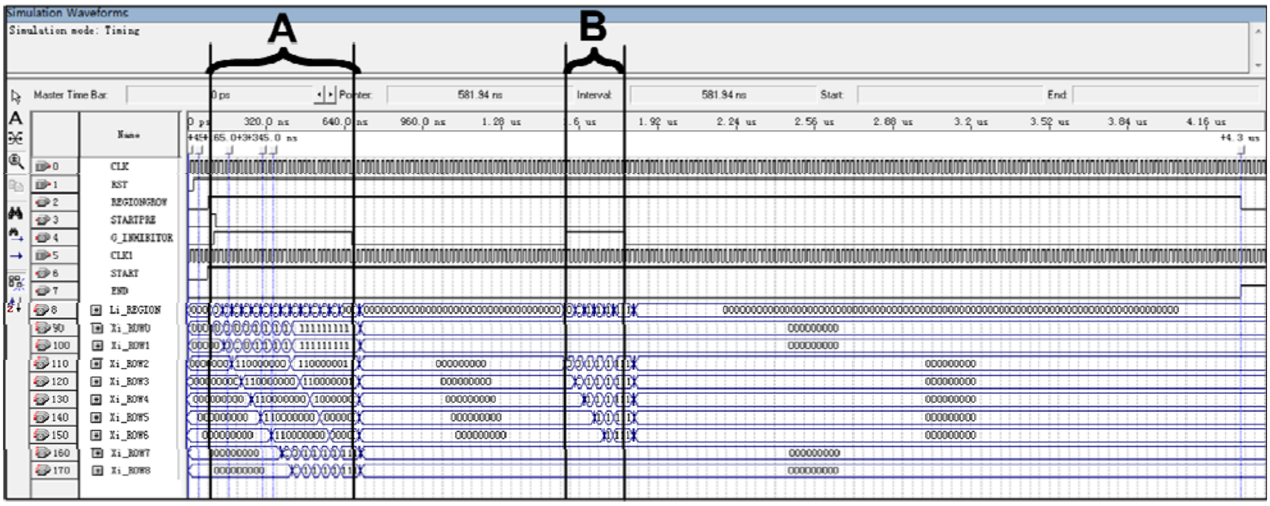

Fig.14 Simulation Result of Image Segmentation Network Module

From the simulation result, it can be seen that the module finishes segmentation of 10x10 image module. The image is segmented into two parts, A and B. Moreover, feature extraction and storage are performed in each segmented region for Li_REGION.

The network cell activation process of regions A and B can be obtained by tracking, as shown in Fig. (15) and Fig.(16):

1	2	3	4	5	6	7	8	9	10
2	2	3	4	5	6	7	8	9	10
3	3							9	10
4	4							10	10
5	5							11	11
6	6							12	12
7	7							13	13
8	8	8	9	10	11	12	13	14	14
9	9	9	9	10	11	12	13	14	15

Fig.15 Network Cell Activation Process in Region A

		1	2	3	4	5	6		
		2	2	3	4	5	6		
		3	3	3	4	5	6		
		4	4	4	4	5	6		
		5	5	5	5	5	6		

Fig.16 Network cell activation process in region B

V. CONCLUSION

Image segmentation is the most important basis of the machine recognition of moving objects, a lot of image segmentation algorithms have been proposed, but with the development of the integrated circuit, an algorithm which can process in real-time with toughness against noise and realize with integrated circuit is needed. This paper proposed a new algorithm, Region Growing-Global Inhibition Segmentation Algorithm (RG-GISA). The main architecture of this algorithm is a cell-network which could realize by digital circuit, and use the concept of LEGION(Locally Excitatory Globally Inhibitory Oscillator Networks)algorithm to realize the end of one region growing and region segmentation, this architecture can realize full-parallel processing of the input image with toughness against noise. Meanwhile, FPGA implementation of this algorithm is realized and the result of simulation is shown in this paper. Compared with the traditional image segmentation algorithm, it can greatly reduce the computation time.

The computation FPGA provides theoretical and technical preparations for future real-time image process and a new method for the implementation of machine mobile object recognition.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflicts of interest.

AKNOWLEDGEMENT

This paper is supported by (Beijing Higher Education Young Elite Teacher Project) YETP1773.

The paper is supported by open project of Beijing Key Laboratory of Information Service Engineering.

This paper is supported by (Funding Project for Academic Human Resourses Development in Beijing Union University)Rx100201510.

The paper is supported byCIT&TCD201304074.

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