Test Scheduling for Network-On-Chip using Zigzag-Type Connected Subgraph Partition

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***Abstract* - The problem of contention for routers and links is one of the critical problems caused by the NoC (network-on-chip) reuse approach in testing NoC systems. In this paper, we propose zigzag connected subgraph partition approach to avoid the contention for routers and links in NoC testing. Then, a MMQEA (multi-population multi-nary quantum-inspired evolutionary algorithm) strategy, which incorporates multi-population and multi-nary techniques, is presented to solve the test scheduling problem for NoC. In addition, power constraint is taken into consideration. Experimental results for the ITC'02 benchmarks show that the new approach results in a reduction in test time, compared to previous work.**

Keywords - Network-on-chip; Test scheduling; Zigzag connected subgraph; Quantum-inspired evolutionary algorithm

I. INTRODUCTION

Nowadays, the riches in electronic consumer market drive designers to use the predesigned and pre-verified embedded cores in complicated system-on-chip (SoC) designs [1]. In SoC, exchanging data between cores are commonly done through a bus-based communication infrastructure. Consequently, higher communication bandwidths, numerous parallel data streams, scalability and global synchronous clock issues are becoming increasingly difficult for a large SoC [2]. It is limited for the current bus-based communication scenario to tackle these problems.

The packet-switched NoC is emerging as a new paradigm in solving the confronted limitations. For systems with a large number of cores and intensive communications load, NoC offers many benefits superior to traditional bus-based architectures [3].

Meanwhile, testing in NoC causes new challenge. Like traditional bus-based SoC, the general issues of NoC testing consist of test wrapper, automatic test equipment (ATE), TAM, and test scheduling [4]. Many test scheduling approaches have been proposed to minimize test cost while satisfy different constraints.

Therefore, an efficient test scheduling method is essential for NoC testing. In [5] E. Cota et al. first proposed the approach of reusing on-chip network as TAM for NoC testing. By adopting the proposed approach, test time minimization can be achieved with minimum area and pin overhead. Due to difference between the speed of NoC functional operating and the speed of core test, J. M. Nolen et al. [6] proposed a time division multiplexed (TDM) strategy to increase test delivery speed, resulting in better test time with lower I/O cost. C. Liu et al. [7] proposed an approach with variable-rate on-chip clocking for test scheduling in NoC under various constraints. M. Richter et al. [8] applied pin-count-aware optimization, pin assignment to access points and core test scheduling, where test time can be decreased for a given pin budget, or the number of test pins can be decreased without influence test time. In [9] M. Agrawal et al. proposed solutions to co-optimize the counts and locations of access points, the ATE distribution to these access points, and the cores assignment to access points for test data delivery.

However, most of these proposed methods suffered from contention for routers and links when transport test vectors and test responses. With contention for routers and links, test time will increase in most cases. These motivate us to adopt disjoint connected subgraph to avoid contention for routers and links in the process of testing. Therefore, our goal is to partition the topology graph into disjoint connected subgraph, and distribute TAM to each subgraph such that the maximum test time of each sub-graph is minimized. In addition, an efficient test scheduling algorithm should be applied to address the NP-complete problem [8].

In this paper, we present a comprehensive test scheduling approach for NoC. The main contributions of this paper are as follows.

We model test optimization problem for the NoC with mesh topology as a connected graph problem and show it is a NP-complete problems.

We refined the QEA with multi-population, multi-nary, named MMQEA. And we apply the MMQEA to solve the scheduling problems.

We take power constraint into consideration in the optimization problem.

In line with prior works, we take time consumption and power consumption in the routers and links into account.

Experimental results with the ITC'02 SoC benchmarks show that, compare to other method, better test time was obtained by our method. Note that, this paper study on the test of the embedded cores.

This paper is organized as follows. In Section 2, we present some basics of NoC scheduling and the definition of zigzag connected subgraph. In Section 3, we briefly explain the concepts of the QEA and MMQEA, and making MMQEA to fit for solving the test scheduling problem. Then, in Section 4, we provide details about the proposed test scheduling algorithm with pseudo-code. Experimental results for the ITC'02 SoC Test Benchmarks are presented in Section 5. Finally, Section 6 concludes the paper.

II. PRELIMINARIES

A. Test strategy

Fig. 1 is a NoC instance of the system d695 from ITC'02 SoC benchmark [10], implementation with a mesh based. The communication channels are defined to be 32-bit wide, and the packets have unlimited length. It uses XY routing, wormhole switching. A packet is broken up into flits (flow control units) which flit size equals the channel width [11]. Each I/O pair connected with test pins of ATE. In Fig. 1, we give one I/O pair to generate test patterns and collect responses from/to the ATE. For example, (C9, C4) is an I/O pair. If C6 (core 6) is assigned to I/O pair (C9, C4), test patterns need to be input from ATE to C9 (core 9) and routed from C8 (core 8) to C6 (core 6), and the test responses of C6 (core 6) be routed to C4 (core 4) and output from C4 (core 4) to ATE. We adopt wrapper design algorithm proposed in [12]. The red solid arrows in Fig. 1 express the dedicated routing paths.

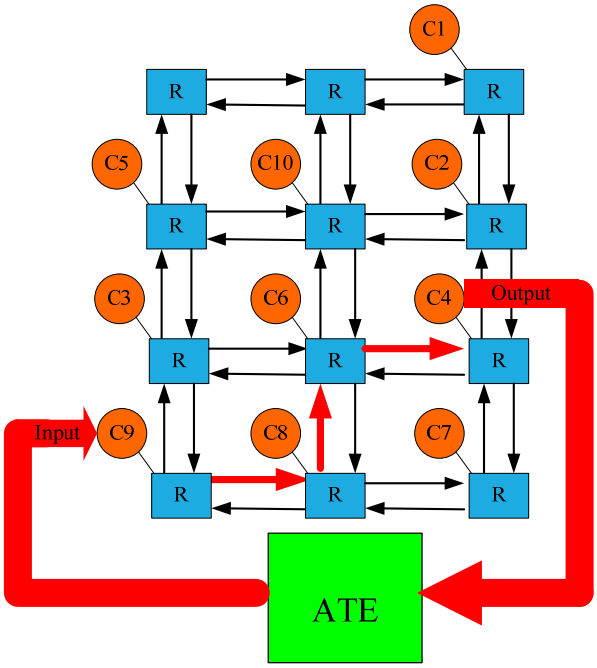

Figure 1. The d695 with a dedicated routing paths.

B. Problem formation

Pzigzagopt: In a NoC system, given the cores Co parameters, the NoC parameters (including n cores, Np I/O pairs (TAM), the network topology, the cores floorplan, routing algorithm etc.), the maximum power limit PL for NoC, decide an zigzag-type connected subgraph partition and a test schedule, such that 1) each core assign only one zigzag-type connected subgraph 2) PL are not violated, and 3) the overall testing time is minimized [7].

This paper designed a test environment: an M*N 2-D mesh topology, reusing NoC as TAM, XY routing, adopting core-based scheduling [5, 13]. In addition, the test must meet the following constraints: Each core in the circuit can be tested only once. Once a core is under test, it can't interrupt and all the test resources on the path are preserved for the core until the entire test process is completed.

C. Coordinates descriptions

A two-dimensional mesh system, denoted as M(md,nd), consists of $m\,d \times nd$ cores (or nodes) arranged in a two-dimensional grid of width m and length n. A node in column I and row j is represented by address <i,j>, for $0 \le i \le md-1$ and $0 \le j \le nd-1$ [14].

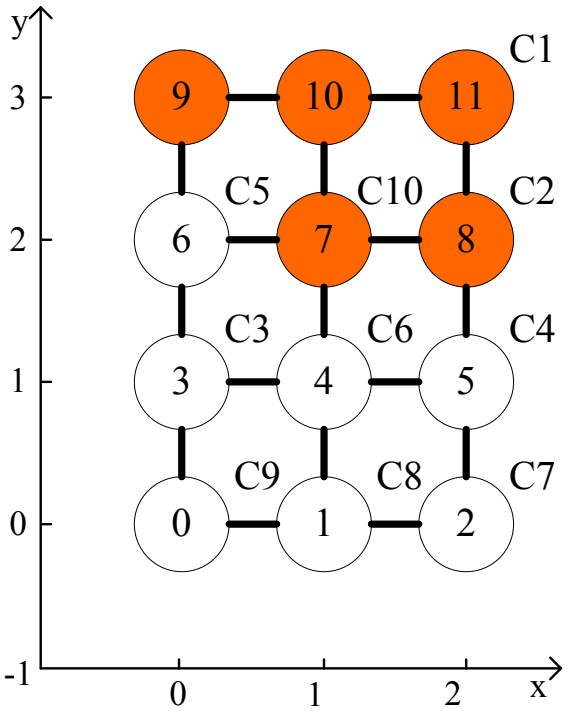

Figure 2. Coordinate model of d695

Definition 1 (zigzag-type connected subgraph). An zigzag-type connected subgraph (ZCS), ZCS(<x1,y1>,<x2, y2>) is the zigzag-type block with start node <x1,y1> and end node <x2,y2>, which is a connected set. It start from <x1,y1> and move along the X-axis direction (or Y-axis direction) to the boundary, and it changes one step direction at Y-axis direction (or X-axis direction). Repeat these steps until reach <x2,y2>. For example, in Fig. 2, a ZCS(<0,3>,<1,2>) subgraph consists of five nodes: 9,10,11,8,7 where node 9 is the start node and 7 is the end node.

Equation (1) defines the relationship of coordinate value and position identity, where PoID is position identity, x is the x-axis coordinate value, y is the y-axis coordinate value, col is the quantity of column. For example, the coordinate value of the position identity '9' is <0,3>.

$$PoID=x+y*col \tag{1}$$

Therefore, for notational simplicity, we can write ZCS(9,7) instead of ZCS(<0,3>,<1,2>).

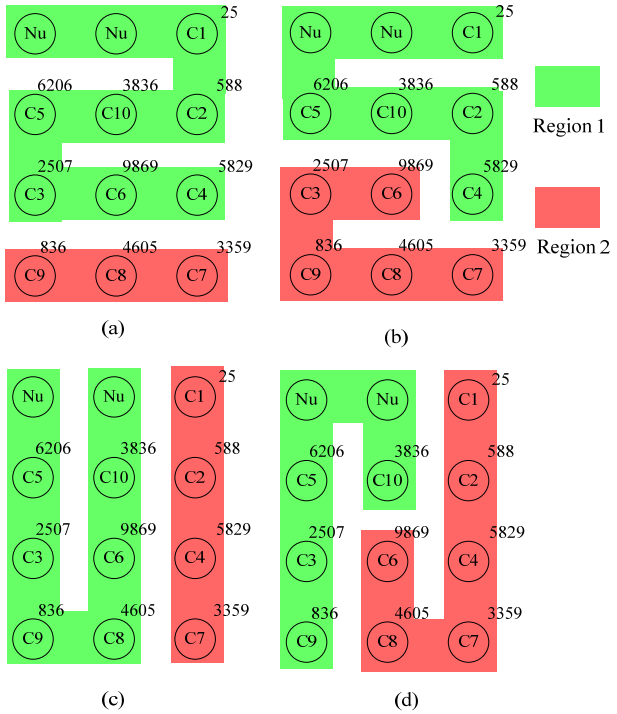

Figure 3. Example of connected subgraph partition result in 4×3 mesh (a) ZHR partition (b) ZHL partition (c) ZVD partition (d) ZVU partition

D. Zigzag-type connected subgraph partition approach

As shown in Fig. 3 (4×3 mesh), we partition the graph into 2 connected subgraph through zigzag line approach. Fig. 3(a) represent ZHR (Zigzag Horizontal Right) partition, (b) represent ZHL (Zigzag Horizontal Left) partition, (c) ZVD (Zigzag Vertical Down) partition, (d) ZVU(Zigzag Vertical Up) partition. We can see from Fig. 3 that different partition can result in different scheduling results.

E. Objective function

The objective function is measured by the test time, as shown in (2).

$$T_{sum} = \max_{1\le j\le B} \sum_{i=1}^{k} T_{testi} \tag{2}$$

where $\sum_{i=1}^{k} T_{testi}$ indicate the time needed to test all cores (number of k) on TAM j. T_{testi} is calculated by (3).

$$T_{testi} = T_{transi} + T_{corei} \tag{3}$$

T_{testi} is the cost time for the i-th core which includes the transmit time T_{transi} and core test time T_{corei}. Equation (4) gives the transmit time for the i-th core.

$$T_{transi} = nb_{ch} * T_{ch} + nb_{r} * T_{r} \tag{4}$$

where T_{ch} indicate the time of the test data consume in the transmit channel, T_r indicate the time consumed in the router, nb_{ch}, nb_r indicate the number of channels and routers, respectively. In line with the previous works, this paper set the transmit channel parameter as follows:$T_{ch} = 0$, $T_r = 3$.

F. Power consumption model

To ensure the viability of the test, the power consumption constraint must satisfy during test.
The total power consumption model is shown in (5).

$$P_{total} = \sum_{i=0}^{tam} P_i \le P_{max} \quad (5)$$

where P_{total} is test total power consumption per cycle, P_{max} is the maximum power consumption allowed for the system, tam is the number of TAM, P_i is the test consumption of TAMi. P_i is calculated by (6).

$$P_i = P_{trani} + P_{corei} \quad (6)$$

where P_{corei} is constant which indicate test power consumption of the core under test on TAM_i. P_{trani} is transmit power consumption of the core under test of TAM_i, including P_{ch} (transmit power consumption in channel) and P_r (power consumption in router). P_{trani} is calculated by (7)

$$P_{transi} = nb_{chi} * P_{ch} + nb_{ri} * P_r \quad (7)$$

where nb_{chi} and nb_{ri} indicate the number of channels and routers of the core under test on TAM_i, respectively. P_{ch} and P_r relates to the given NoC system. In [11] E. Cota et al. give the definition of P_{ch} and P_r. In line with previous results, we assume $P_{ch} = 2$、$P_r = 10$.

III. MMQEA

In 2002, H. Kuk-Hyun et al. [15] proposed QEA (quantum-inspired evolutionary algorithm), which possesses of small population, fast convergence and good global search capability. However, the QEA is mainly applied in the binary problem as it only has two quantum states. While for non-binary problem, it requires a large number of binary qubits to represent the problem solution.

As the NoC test scheduling problem just is not a simple binary problem, it is necessary to improve the encoding of QEA and make it suitable for NoC test scheduling problem. This paper refers to multi-nary compound states of probability angle coded quantum-inspired evolutionary algorithm [16], which extends the classic two states of a quantum bit into multiple states and directly solves the non-binary optimization problem. In order to solve the premature convergence problem of the classic QEA and obtain a balance between exploration and exploitation, refer to multi-population in the natural evolution, this paper proposes MMQEA to solve the NoC test scheduling problem.

The process of the MMQEA is similar to the process of classic QEA [15]. We use probability angle to replace probability amplitude to denote multi-nary states. And the MMQEA is re-defined as follows.

A. Encoding

We extend the basic binary to multi-nary, using $\varphi_1, \varphi_2, \cdots, \varphi_m$ as multi-nary code. A new Q-bit can be represented as
$[\varphi_1, \varphi_2, \cdots, \varphi_m]^T$, $\varphi_1 + \varphi_2 + \cdots + \varphi_m = 45 \times M$, and $0 < \varphi_1, \varphi_2, \cdots, \varphi_m < 45 \times M$

The $Q(t) = \{q_1^t, q_2^t, \cdots q_n^t\}$ is a population of Q-bit individuals at generation t, where n is the size of population. An individual based on MMQEA is described in (8).

$$q_z^t = \begin{bmatrix} \varphi_{11}^t & \varphi_{12}^t & \cdots & \varphi_{1N}^t \\ \varphi_{21}^t & \varphi_{22}^t & \cdots & \varphi_{2N}^t \\ \cdots & \cdots & \cdots & \cdots \\ \varphi_{M1}^t & \varphi_{M2}^t & \cdots & \varphi_{MN}^t \end{bmatrix} \quad (8)$$

B. Updating operation

For multi-nary, updating is mainly to change the probability of observing 0,1,2,…,M-1. So the probability angle φ_x decreasing or increasing is equivalent to probability amplitude affected by the rotation gate. When performing updating operation, if the probability angle corresponding to observing value decreases with $\Delta\theta$, the probability angle corresponding to the best solution increases with $\Delta\theta$, guaranteeing the updated angle non-negative.
If $\varphi_x - \Delta\theta > 0$ then $\varphi_x' = \varphi_x - \Delta\theta$, $\varphi_b' = \varphi_b + \Delta\theta$
If $\varphi_x - \Delta\theta < 0$ then $\varphi_x' = \Delta\theta - \varphi_x$, $\varphi_b' = \varphi_b - \Delta\theta + 2\varphi_x$

where, $\Delta\theta$ express rotation angle, φ_b and φ_b' express probability angle corresponding to the best solution last

generation and current generation, respectively. The φ_x express the probability angle corresponding to the observing value. The magnitude of rotation angle $\Delta\theta$, which can be changed by the observing value of individual x_j^t and the best individual value b_j^t, can be obtained by lookup table.

C. Observing operation

The value of observing operation is an integer. Generating a random $r \in [0,45 \times B]$, according to the position of which lies in to decide the observing value. For example, if r=96, B=4, $\varphi_1 + \varphi_2 < r < \varphi_1 + \varphi_2 + \varphi_3$, then the observing value is 2.

D. Multi-population

The basic idea of multi-population in QEA is to use two or more subpopulation instead of the traditional single population. In traditional QEA, single population can only use single operation strategy in the process of evolutionary. Instead, multi-population can adopt different operation strategy for different subpopulations. The advantages of multi-population in QEA are that each population evolved independently, ensures the diversity of population, fundamentally overcomes the problem of premature in traditional QEA, and information exchange between the population increased convergence speeds.

IV. TEST SCHEDULING FOR NOC USING MMQEA

A. Integer vector coding and definition

Define 2: $\forall T_k \in PV^n$, $k \in [1, N]$, N is the population size, n is the number of fitness variable, H_k is an observing individual, $T_k = (PV_1, PV_2, \cdots PV_n)$ is a feasible solution to problems, denote an assignment of IP core to TAMs.

Define 3: For observing variable PV, $\forall PV$, $i \in [1, N]$, $PV_i \in C$, C is an integer set. Define C={1, 2,..., Np}, where Np is the number of TAMs.

Suppose there are n IP core under test, Np TAM, the t-th generation group of assignment test data to the TAM are $Q(t) = \{q_1^t, q_2^t, \cdots q_n^t\}$, n is the size of the population. Eq. (8) is a test data distribution scheme using quantum coding, namely the code of the z-th individual.

In the coding scenario, the Q-bits are the genes of individual. The n Q-bits denote assignment of n IP core to TAMs. Each Q-bit has Np quantum states, namely denote there is Np TAMs. Assuming IP core under test n = 10, TAMs Np = 4, by observing quantum coding of the individual, we can get 4-nary strings of length 10. For example, if we get "1120330020", we rearrange it to "0000112233" , denote core with PoID 1,2,3,4 are assigned to TAM1, 5,6 to TAM2, 7,8 to TAM3, 9,10 to TAM4, respectively.

B. MMQEA for the test scheduling problem

MMQEA for the test scheduling problem consists of a basic structure of QEA and other processes to satisfy the NoC characteristics. The algorithm can be described in Fig. 4 [15].

t=0

(1) initialize quantum population Qa(0) and Qb(0)

(2) generate Pa(0) and Pb(0)by observing the states of Qa(0)and Qb(0), respectively

(3) NoC_schedule_Zigzag

(4) evaluate Pa(0) and Pb(0), respectively

(5) save the best solutions among Pa(0) and Pb(0) into Ba(0) and Bb(0), respectively

while (not end condition) do

t=t + 1

(6) generate Pa(t) and Pb(t) by observing the states of Qa(t -1) and Qb(t -1), respectively

(7) NoC_schedule_Zigzag

(8) evaluate Pa(t) and Pb(t), respectively

(9) update Qa(t) and Qb(t) using Q-gates, respectively

(10) save the best solutions among Ba(t-1) and Pa(t) into Ba(t), Bb(t-1) and Pb(t) into Bb(t), respectively

(11) save the best solution ba and bb among Ba(t) and Bb(t), respectively

(12)if (migration-period)

then migrate N individuals between Qa(0) and Qb(0)

Figure 4. Procedure MMQEA for the test scheduling problem

For each an assignment of core to TAM (corresponded to an individual), we place the unscheduled core to TAM for testing until all cores are test finished. In addition, power

constraint is satisfied during testing. In order to test efficiently, we set the position of the input and output ports using the start node and end node of each connected subgraph. The detailed pseudocode of the proposed power-aware test scheduling procedure using zigzag-type connected subgraph is shown in Fig. 5.

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(1)Assume the number of unscheduled cores is unCount
(2)Set tsequence =0    /*test timing sequence*/
(3)Upon an assignment of core to TAM(a string of Q-bits)
(4) While unCount!=0
(5) Record the position of recent free TAM
(6) For each TAM
(7) Find an available TAM;
(8) If no available TAM
(9) Update tsequence;
(10)  unCount = unCount -1;
(11) else
(12) if all core assign to one TAM are test finished
(13) label the TAM is unavailable;
(14)  else
(15) Find an unscheduled core assign to this available TAM;
(16)  If total power limit is not exceeded
(17)    Place the unscheduled core to TAM;
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Figure 5. Procedure NoC_schedule_Zigzag.

V. EXPERIMENTAL RESULTS

In this section, we used three SOCs from the ITC'02 SoC Test Benchmarks [10], namely, d695, p22810 and p93791, with 10, 28 and 32 cores, respectively. For the sake of comparison, we assumed the NoC with the same configurations, as those used in [17]. Meanwhile, the power consumption statistics were adopted from [18]. A percentage of the total power consumption of all cores in test mode is defined to the power consumption limit for the system [13]. For instance, 50% power limit represents that the power limit is equal to 50% of the sum of the power consumption of all cores under test. All the results were obtained on an Intel (R) Core (TM) machine with 3.1Ghz processor and 3G RAM.

Figs. 6-8 compare the test time (y-axis) for our method and [17] under different power constraints, on different numbers of I/O ports (TAMs) (x-axis). Fig. 6-8 give the results for the d695, p22810 and p93791 benchmarks, respectively.

It can be observed from Figs. 6-8, our method is more efficient than [17] . A test time reduction is gained with and without power constraints, on different numbers of I/O ports. In most cases, it can also be seen that the test time will increase when adding a power constraint. But in some cases, test time may not be affected for the loose power constraint. It can also be seen that, in all cases, the decrease in test time can lead to the increase in the number of ports.

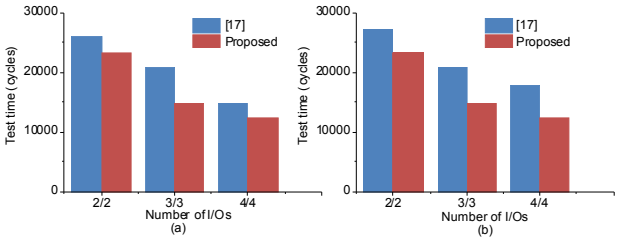

Figure 6. Test time comparison of our method and [17] for d695 (a) No power limit (b)50% power limit.

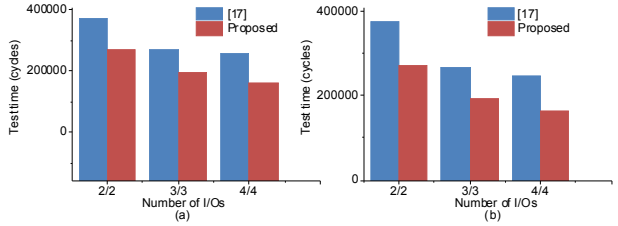

Figure 7. Test time comparison of our method and [17] for p22810 (a) No power limit (b) 50% power limit.

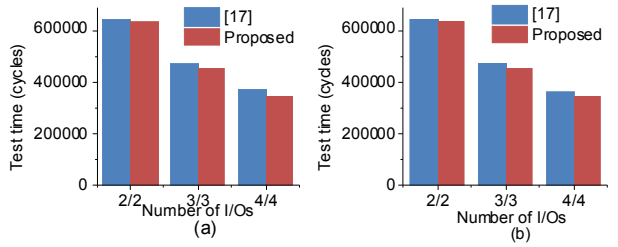

Figure 8. Test time comparison of our method and [17] for p93791 (a) No power limit (b) 50% power limit.

VI. CONCLUSION

This paper has proposed a novel approach for NoC test scheduling. In the method of reusing the on-chip network as TAM in NoC, contention for routers and links is a significant influence factor in test cost. Thus, zigzag-type connected subgraph partition approach was proposed to address the problem. The MMQEA was presented to solve the test scheduling problem which proved to be NP-complete problem. Experimental results on ITC'02 benchmark circuits showed that the proposed approach can lead to a reduction in test time. Consequently, since the

proposed scheduling approach proves to be very effective and feasible for testing NoC, we expect further related research will be encouraged.

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REFERENCES

[1] V. Iyengar and K. Chakrabarty, "System-on-a-chip test scheduling with precedence relationships, preemption, and power constraints," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, pp. 1088-1094, 2002.

[2] L. Benini and G. De Micheli, "Networks on chips: a new SoC paradigm," Computer, vol. 35, pp. 70-78, 2002.

[3] C. Zeferino, M. Kreutz, L. Carro, and A. Susin, "A Study on Communication Issues for Systems-on-Chip," in *Proceedings of the 15 th Symposium on Integrated Circuits and Systems Design*, 2002, pp. 121-126.

[4] A. M. Amory, C. Lazzari, M. S. Lubaszewski, and F. G. Moraes, "A new test scheduling algorithm based on Networks-on-Chip as Test Access Mechanisms," *Journal of Parallel and Distributed Computing*, vol. 71, pp. 675-686, 2011.

[5] E. Cota, M. Kreutz, C. A. Zeferino, L. Carro, M. Lubaszewski, and A. Susin, "The impact of NoC reuse on the testing of core-based systems," in *Proceedings of the 21st IEEE VLSI Test Symposium*, 2003, pp. 128-133.

[6] J. M. Nolen and R. Mahapatra, "A TDM Test Scheduling Method for Network-on-Chip Systems," in *Proceedings of the Sixth International Workshop on Microprocessor Test and Verification*, 2005, pp. 90-98.

[7] C. Liu, V. Iyengar, J. Shi, and E. Cota, "Power-aware test scheduling in network-on-chip using variable-rate on-chip clocking," in *Proceedings of the 23rd IEEE VLSI Test Symposium*, 2005, pp. 349-354.

[8] M. Richter and K. Chakrabarty, "Optimization of Test Pin-Count, Test Scheduling, and Test Access for NoC-Based Multicore SoCs," *IEEE Transactions on Computers*, vol. 63, pp. 691-702, 2014.

[9] M. Agrawal, M. Richter and K. Chakrabarty, "Test-Delivery Optimization in Manycore SOCs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, pp. 1067-1080, 2014.

[10] E. J. Marinissen, V. Iyengar and K. Chakrabarty, "A set of benchmarks for modular testing of SOCs," in *International Test Conference*, 2002, pp. 519-528.

[11] E. Cota, L. Carro, F. Wagner, and M. Lubaszewski, "Power-aware noc reuse on the testing of core-based systems," in *International Test Conference*, 2003, pp. 612-621.

[12] V. Iyengar, K. Chakrabarty and E. J. Marinissen, "Test Wrapper and Test Access Mechanism Co-Optimization for System-on-Chip," *Journal of Electronic Testing: Theory and Applications*, vol. 18, pp. 213-230, 2002.

[13] E. Cota and C. Liu, "Constraint-Driven Test Scheduling for NoC-Based Systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, pp. 2465-2478, 2006.

[14] G. Chiu and S. Chen, "An efficient submesh allocation scheme for two-dimensional meshes with little overhead," *IEEE Transactions on Parallel and Distributed Systems*, vol. 10, pp. 471-486, 1999.

[15] H. Kuk-Hyun and K. Jong-Hwan, "Quantum-inspired evolutionary algorithm for a class of combinatorial optimization," *IEEE Transactions on Evolutionary Computation*, vol. 6, pp. 580-593, 2002.

[16] S. SHEN and W. JIN, "Multinary Compound States of Probability Angle Coded Quantum-Inspired Evolutionary Algorithm," *Pattern Recognition and Artificial Intelligence*, vol. 18, pp. 657-663, 2005.

[17] É. Cota, L. Carro and M. Lubaszewski, "Reusing an on-chip network for the test of core-based systems," *ACM Transactions on Design Automation of Electronic Systems*, vol. 9, pp. 471-499, 2004.

[18] J. Pouget, E. Larsson and Z. Peng, "SOC test time minimization under multiple constraints," in *Proceedings of the 12th Asian Test Symposium*, 2003, pp. 312-317.