CMOS Bridge Rectifier (CBR) using 0.18 Micron Technology for Energy Harvesting Applications

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Abstract - **In this work, an input-powered AC/DC CMOS bridge rectifier (CBR) is proposed using 0.18 μm CMOS process. It is based on a simple bridge connected full wave rectifier, without an external dc voltage to turn-ON. The rectifier may be used for energy harvesting applications with a typical output of relatively low-amplitude input and low frequency of ac voltages. The proposed CBR achieves a maximum voltage efficiency of 96% with 1.0-V ac input amplitude and 50 Hz input frequency, delivering 1.22 mW of output power. The proposed CBR occupies an active area of 0.0054 mm2 that is at least 58.5 % smaller than other reported solutions.**

Keywords - Bridge-Rectifier; CMOS; Energy-Harvesting; Input-Powered; Miniaturized.

I. INTRODUCTION

The ever-increasing demand for portable and lightweight electronic devices has led to the decrease in the supply voltage magnitude requirement, which is dependent on batteries as a source of energy. The drawback in terms of the need for regularly charging or replacing batteries may be alleviated through the use of micro energy harvesters, resulting in lightweight and compact systems [1][2]. For that, a harvester requires converter AC to DC circuits to transform the generated alternate energy (normally in AC or RF form) into electrical energy of usable form (normally in DC form) [3][4].

A good rectifying circuit in this case needs to be chosen based on the suitability of its topology and its technology of implementation for mobile applications, i.e., lightweight, compact and efficient. Due to their inherent very low voltage applications (<3.0V), a low on-state resistance with associated low voltage drop are desirable characteristics for the system to be feasible. Thus, typical MOS diodes or even discrete Schottky diodes must be averted.

Many rectifier topologies have been reported since the proliferation of mobile applications; the simplest being the full-bridge rectifier with CMOS technologies for higher efficiencies with a reduction in a voltage drop. Other effort to reduce the size has seen work on 0.5 μm CMOS process [5] with the size of 0.013 mm2. Further reduction in size becomes apparent when 0.35 μm CMOS process was involved [6], leading to 0.007 mm2 area size.

In this work, an input-powered AC/DC CMOS bridge rectifier is proposed using 0.18 μm CMOS process. It is based on a simple bridge-connected full wave rectifier, without an external dc voltage to turn-ON. The rectifier may be used for energy harvesting applications with a typical output of relatively low-amplitude input and low frequency of ac voltages [7].
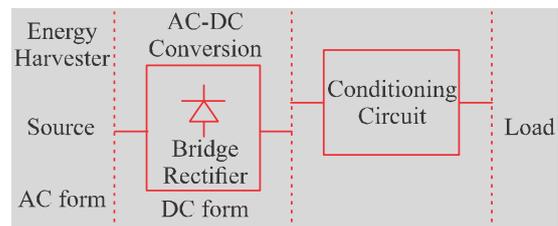
II. TYPICAL ENERGY HARVESTER SYSTEM

Figure 1. Block diagram of an energy harvesting system (EHs)

Figure 1 depicts the block diagram of an energy harvesting system (EHs). It comprises three (3) major elements: a) source from energy harvester, b) AC-DC conversion block, and c) Conditioning Circuit that may include voltage booster, storage devices, filter and control circuits, etc. [8]. In most cases, electrical energy is converted from several alternative energy harvesters in the form of piezoelectric, inductive and capacitive generators.
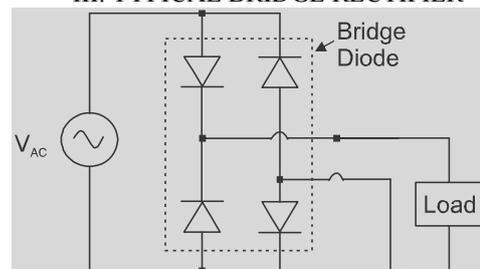
III. TYPICAL BRIDGE RECTIFIER

Figure 2. Conventional bridge rectifier (BR) employing diodes

Typical high quality full-wave AC/DC rectifier uses a bridge topology employing 4 diodes as shown in Figure 2. However, the diode rectifier with high forward voltage drop (typically in the range of 0.7 V to 1.0 V) would reduce the power efficiency of the converter when implemented in low-voltage circuit. The output power and voltage in low power applications such as energy harvester devices are usually low, often only in microwatt to milli-watt range, necessitating voltage- and power-efficient converters.
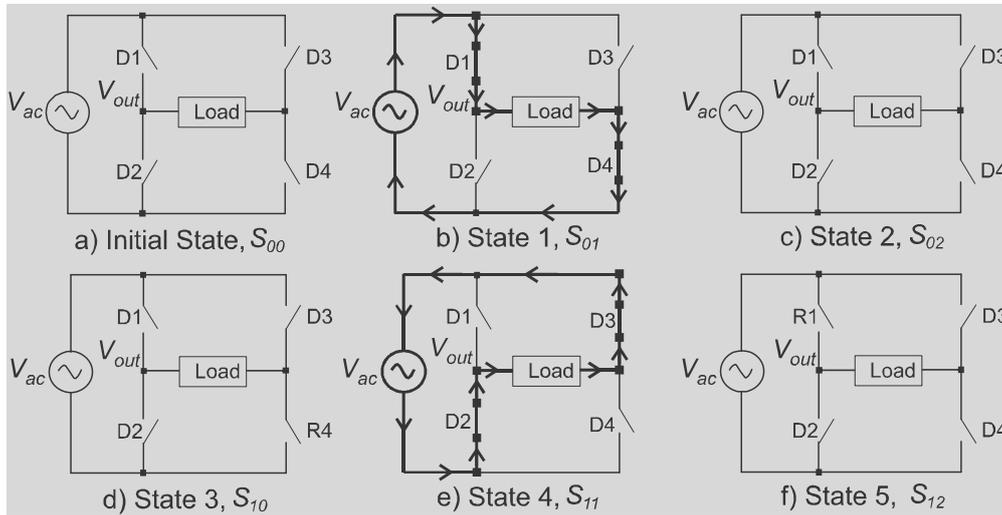

Fig. 3. Switching sequence of diode-based BR in six switching states

Fig. 3 shows the switching sequences of the BR in six (6) states of operation. Note that, the diode is operating as a switch, thus the diodes in BR are turned on when Vac > Vth_diode, which is 0.7 V. Therefore, the input ac voltage must be bigger than 0.7 V to switch on the diode. The diodes are arranged in the different polarity to develop the full-wave rectifier sequences as shown in Fig.3(a).

From BR equivalent circuit, the voltage drop is leading the losses in the output voltage. Thus, the output voltage, Vout in the positive half-cycle of the input AC voltage in the rectifier circuit can be obtained using the following relationship:

$$V_{out} = V_{AC} - V_{drop\_D1} - V_{drop\_D4} \qquad (1)$$

where V_{ac} is the AC voltage amplitude of the sinusoidal signal, while V_{drop_D1} and V_{drop_D4} represent the losses of diodes in BR. From equation (1), the input ac voltage, V_{ac} must be bigger than $2*V_{drop\_D}$, which is 1.4 V.

Then, the output power, P_{out} and efficiency, η of the BR are given as [9]:

$$P_{out} = V_{out}^2 / R_{load} \qquad (2)$$

$$P_{in} = 1/T \int_0^T \left(V_{in}(t) \times I_{in}(t) \right) dt \qquad (3)$$

From (2) and (3), the overall system efficiency is obtained as:

$$\eta = P_{out} / P_{in} = V_{out}^2 / R_{load} \times T / \int_0^T \left(V_{in}(t) \times I_{in}(t) \right) dt \qquad (4)$$

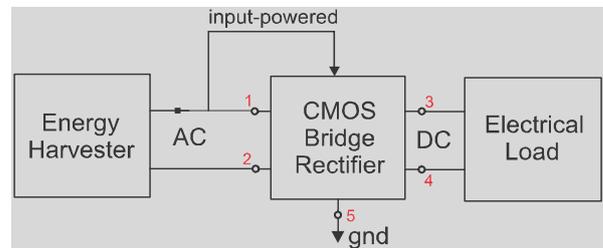## IV. PROPOSED CMOS BRIDGE RECTIFIER (CBR)

Fig. 4 Block diagram of proposed CMOS bridge rectifier (CBR)

To reduce the rectifier size, a single-stage CMOS Bridge Rectifier (CBR) is proposed as depicted in Fig. 4. It is implemented using 0.18-micron CMOS process technology; powered by its input AC voltage. It has only five (5) external connections; two (2) for the input, two (2) for the output and one (1) connected to ground (gnd).

The proposed CBR is targeted for low input AC voltage with an output DC voltage with low voltage drop. The working frequency is set at 50 Hz input with 1.0 V input ac voltage of operation. The proposed CBR functions to convert AC input voltage to a DC output.
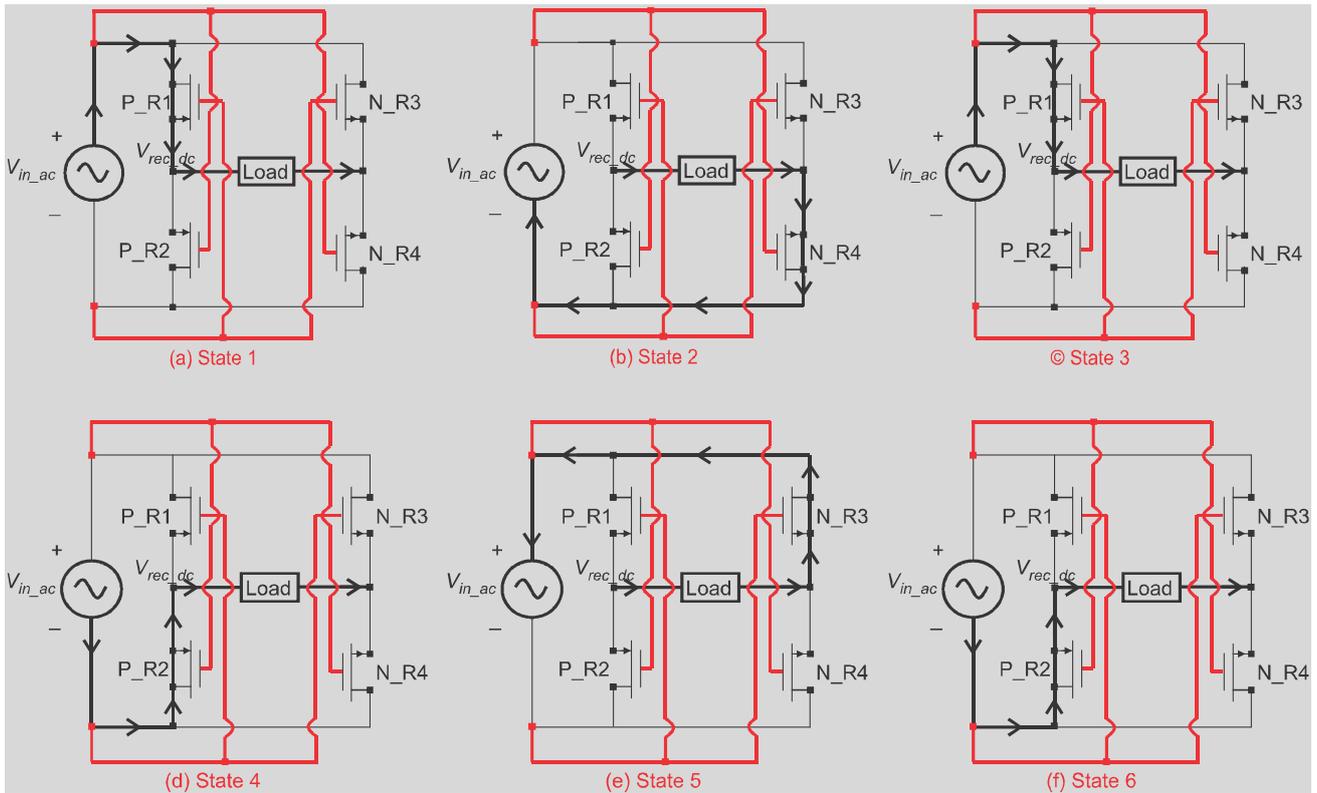
Fig. 5 Switching sequence of CBR in six switching states.

Fig. 5 (a to f) shows the switching sequences of the CBR in six states of operation with switching algorithm defined in Table 1. The turning ON and OFF of the MOSFETs (R1 to R4) are based on the different potential of the gate-source voltage, Vgs and the threshold voltage, Vth_MOS. Note that, the NMOS is turned ON only when Vgs > Vth_MOS _NMOS while PMOS is turned ON only when Vgs < Vth_MOS _PMOS.

TABLE 1: CBR SWITCHING ALGORITHM OF MOSFETS IN THE DIFFERENT STATES

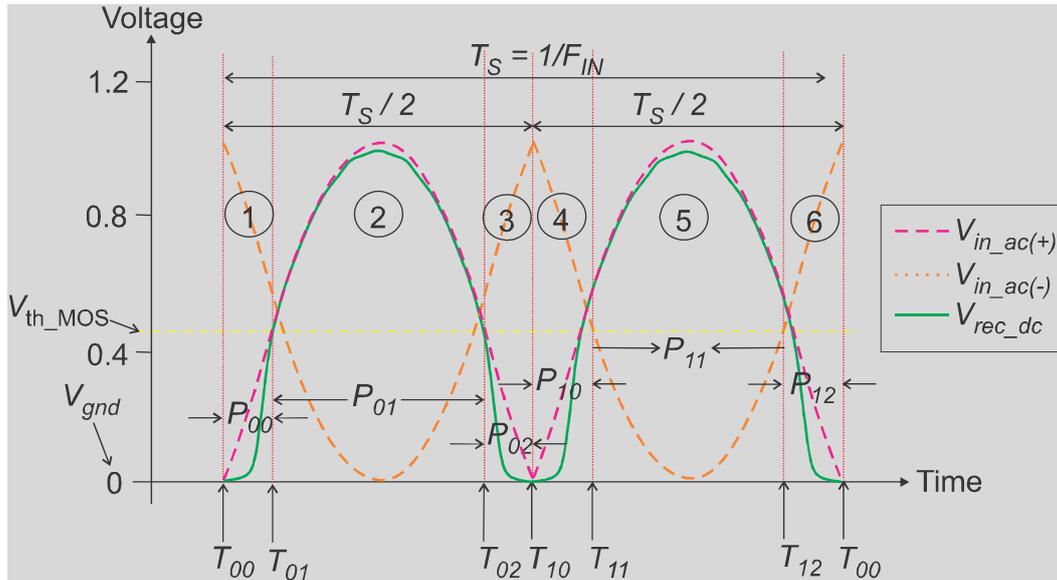| Condition	State	Period	Time	R1 PMOS	R2 PMOS	R3 NMOS	R4 NMOS
$V_{in\_ac(+)} > V_{in\_ac(-)}$	1	P_{00}	$T_{00} < t < T_{01}$	ON	OFF	OFF	OFF
	2	P_{01}	$T_{01} < t < T_{02}$	OFF	OFF	OFF	ON
	3	P_{02}	$T_{02} < t < T_{10}$	ON	OFF	OFF	OFF
$V_{in\_ac(+)} < V_{in\_ac(-)}$	4	P_{10}	$T_{10} < t < T_{11}$	OFF	ON	OFF	OFF
	5	P_{11}	$T_{11} < t < T_{12}$	OFF	OFF	ON	OFF
	6	P_{12}	$T_{12} < t < T_{00}$	OFF	ON	OFF	OFF

31.3

Fig. 6. Voltage waveform over one cycle of CBR

Fig. 6 shows the simulated waveforms of input ac voltages; Vin_ac(+) and Vin_ac(-), together with Vrec_dc and VGND for the CBR circuit. Note that, the period of time from P00 to P02 for positive cycle of input ac source, while P10 to P12 for negative cycle of input ac source in CBR circuit.

At the initial of the period t = T00, when Vin_ac(+) = 0 and Vgs of the MOSFETs are zero, thus the MOSFETs P_R1, P_R2, N_R3, and N_R4 in CBR circuit are turned OFF. When Vin_ac(+) > 0 in state 1, the Vgs of the P_R1 is smaller than Vth_MOS, thus the P_R1 is turned ON. Meanwhile, the N_R4 is turned OFF due to Vgs < Vth_MOS. At t = T01 when Vin_ac(+) > 0, Vgs of the N_R4 is higher than Vth_MOS, thus the N_R4 is turned ON. During the interval, the P_R1 is turned OFF due to Vgs > Vth_MOS. However, the Vin_ac(+) is reduced after reaching the peak voltage at 1.0 V in state 2. Thus, at T = T02 when Vin_ac(+) > 0, Vgs of the N_R4 is smaller than Vth_MOS, caused the N_R4 to turn OFF. Meanwhile, the P_R1 is turned ON due to Vgs < Vth_MOS in state 3. In state 1, 2 and 3 the MOSFETs P_R2 and N_R3 are turned OFF due to the reverse-biased condition.

The operation of the CBR in the second half-cycle is similar to the first half-cycle, except that P_R2 and N_R3 are turning ON. When Vin_ac(-) > 0 in state 4, the Vgs of the P_R2 is smaller than Vth_MOS, thus the P_R2 is turned ON. Meanwhile, the N_R3 is turned OFF due to Vgs < Vth_MOS. At t = T11 when Vin_ac(-) > 0, Vgs of the N_R3 is higher than Vth_MOS, thus the N_R3 is turned ON. During the interval, the P_R2 is turned OFF due to Vgs > Vth_MOS. However, the Vin_ac(-) is reduced after reaching the peak voltage at 1.0 V in state 5. Thus, at T = T12 when Vin_ac(-) > 0, Vgs of the N_R3 is smaller than Vth_MOS, caused the N_R3 to turn OFF. Meanwhile, the P_R2 is turned ON due to Vgs <

Vth_MOS in state 6. In state 4, 5 and 6 the MOSFETs P_R1 and N_R4 are turned OFF due to the reverse-biased condition.

V. SIMULATION MODEL

In contrary to conventional full-wave rectifier topology, MOSFETS are used instead of diodes in the design. These MOSFETs reduce the undesirable power loss during forward bias due to the higher ON-state resistance associated with diodes; a constraint for low input AC voltage of AC-DC converter using CMOS technology [11]. However, the design of an equivalent rectifier based on MOSFET must consider other constraints due to the inherent drawback that includes: high leakage, low gate oxide breakdown, and larger area requirements. The proposed MOSFETs require large value of W with the value of constant k1, to achieve feasible Id. Thus, the threshold voltage Vth of the MOSFETs is reduced. An increase in the output power capacity and improvements in efficiency is expected.

The drain current gives the relationship between the threshold voltage and the size of W and L, I_d, equation [12]:

$$I_d = \frac{k_1}{2} \times (W/L) \times (V_{gs} - V_{th})^2 \qquad (5)$$

The dependence of drain current follows equation (5) to determine the size of MOSFETs required, taking into account the need to minimize the voltage drop and to increase the output power of the rectifier.

From (5), the size of W can be written as:

$$W = \frac{2L \times I_d \times T_{ox}}{\mu_n \times \varepsilon_0 \times \varepsilon_r \times \left(V_{gs} - V_{th}\right)^2} \qquad (6)$$

where, μ_n represents the surface electron mobility, while $(\varepsilon_0 \times \varepsilon_r)$ is known as permittivity of silicon dioxide and T_{ox} is the gate oxide thickness [13]. The size of L is constant at the minimum channel length, 0.18 μm.

The threshold voltage of the MOSFET is given by:

$$V_{th} = VTO + KT1\left(\frac{T+273}{Tref} - 1\right) \qquad (7)$$

where *VTO* is the zero-bias of threshold voltage, *KT1* is the temperature coefficient for threshold voltage, *T* is the default temperature and T_{ref} is the reference temperature of the model MOS device.

In schematic design, the *W* size of MOS devices, NMOS and PMOS were determined using equation (6). Subsequently the threshold voltage, V_{th_MOS} of MOS devices, NMOS and PMOS were formulated using equation (7). Table 2 shows a compilation of the *W* size of MOSFETs in CBR circuit.

TABLE 2: W SIZE OF MOSFETS IN CBR CIRCUIT

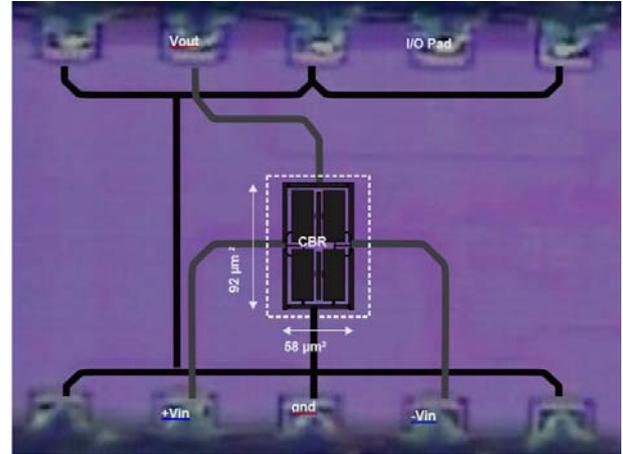| MOSFET	Type	*W/L* Ratio
P_R1, P_R2	PMOS	750/0.18
N_R3, N_R4	NMOS	750/0.18

VI. IMPLEMENTATION OF CBR

Fig. 8. Die photo and detailed view for the CBR

The proposed CBR circuit was designed and fabricated using 0.18 μm CMOS technology with the micrograph as shown in Fig. 8. The total active area for CBR circuit was 0.0054 mm2 (93 μm x 58 μm). The I/O pads without ESD protection were used instead of ESD diodes to avoid short circuiting of input AC signal. The size I/O pad was 0.0025 mm2 (50 μm x 50 μm) and the size between two I/O pads was 50 μm.
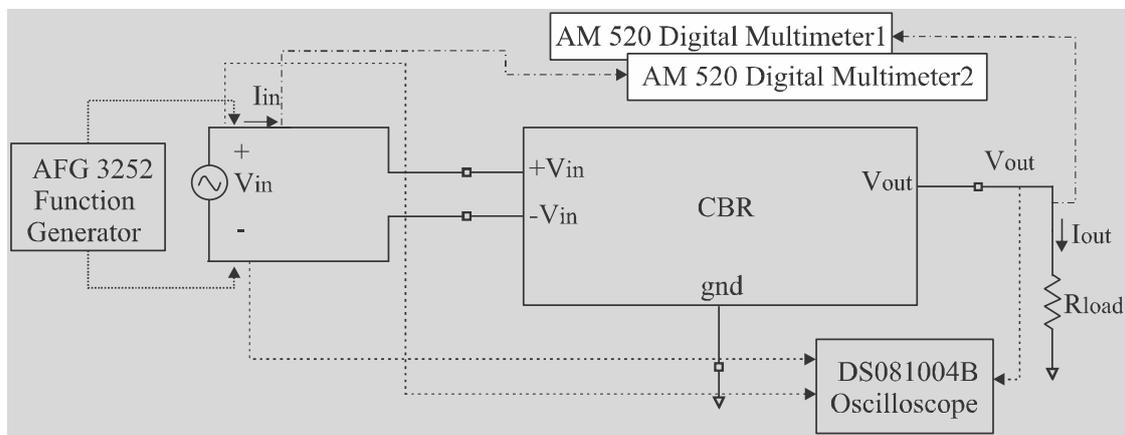

Fig. 9. Block diagram of the experimental setup for CBR circuit

Fig. 9 presents the block diagram of the experimental setup for CMOS bridge rectifier, CBR circuit. The function generator, Tektronix AFG 3252 provides an ac input voltage, Vin to the CBR circuit, which generates the dc output voltage, Vout_dc for load resistance, Rload. The input and output currents were measured with the two Amprobe AM 520 digital multimeters. The input ac and output dc voltages were displayed using a Agilent DS081004B oscilloscope.

VII. RESULTS AND DISCUSSION

A. Simulation Results of CBR

The characteristics of the CBR circuit in terms of electrical performances i.e. voltage efficiency and voltage drop with respect to the variation of the external parameters i.e. Vin, Fin and Rload are presented. In the first scenario, the effect of input voltage parameter, Vin to

the electrical performance was observed. Four sets of input voltages were chosen, which are 0.5 V, 1.0 V, 1.5 V and 2.0 V, while Fin and Rload are fixed at 50 Hz and 500 Ω, respectively. The minimum input voltage is set to 0.5 V which limited by the threshold voltage of the MOSFETs in the CBR. While the maximum input voltage is set to 2.0 V which considered not to beyond the gate-oxide breakdown voltage of the 0.18 μm CMOS technology.
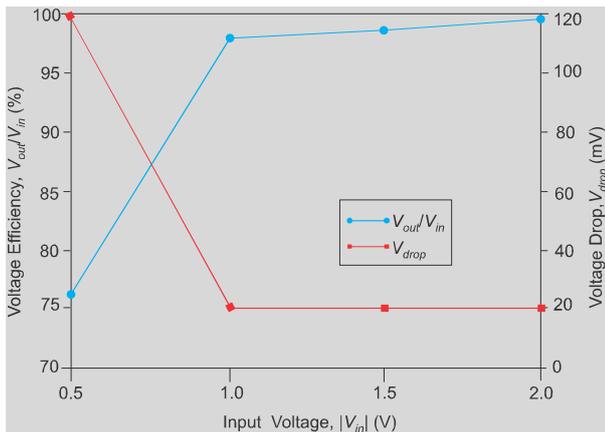

Fig. 10. Simulated voltage efficiency, Vout_dc/Vin_ac and voltage drop, Vdrop versus input voltage

The voltage efficiency, % Vout_dc/Vin_ac and voltage drop, Vdrop for CBR circuit are simulated as shown in Fig. 10. It is seen that the input voltage Vin has clearly influence on the voltage efficiency as well as the voltage drop of the CBR circuit. As the input voltage Vin increased, the voltage efficiency increased to the optimize voltage efficiency while the voltage drop Vdrop decreased. However, the different of the voltage efficiency and voltage drop between the varied input voltages at 1.0 V to 2.0 V were minimal.
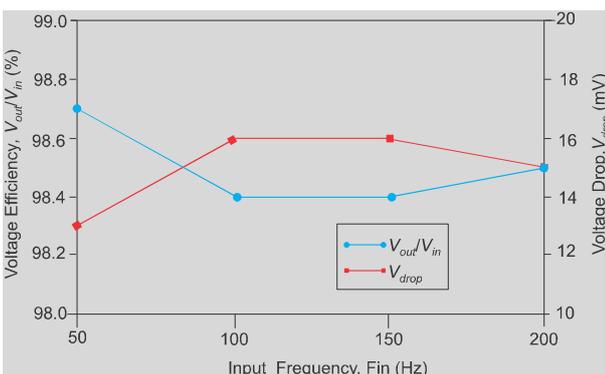

Fig. 11. Simulated voltage efficiency, Vout_dc/Vin_ac and voltage drop, Vdrop versus input frequency

In the second scenario, the effect of input frequency parameter, Fin to the electrical performance of the CBR circuit was observed. Four sets of input frequencies were chosen, which are 50 Hz, 100 Hz, 150 Hz and 200 Hz,

while Vin and RLoad are fixed at 1.0 V and 500 Ω, respectively. The range of the input frequency is limited by the ac input frequencies from micro harvester generator which used previously.

It can be seen in Fig. 11, the simulated voltage efficiency and voltage drop of CBR circuit for all four different sets of input frequencies have shown variation of electrical performances. As Fin increases from 50 Hz to 150 Hz, the voltage efficiency reduced while the voltage drop increased. As such, it can be inferred that, Fin influences the voltage efficiency as well as the voltage drop of CBR circuit. However, the different of the voltage efficiency and voltage drop between the varied input frequencies were minimal.

Finally, the third scenario will see the effect of parameter load resistance, Rload on the electrical performance of CBR circuit when it was varied. Four different sets of value for Rload were chosen given by 0.5 kΩ, 1.0 kΩ, 1.5 kΩ and 2.0 kΩ while Vin and Fin are fixed at 1.0 V and 50 Hz, respectively. The minimum Rload is limited by the expected current flow through MOSFETs which discussed in previous chapter. Larger Rload decrease the output power of the CBR circuit.
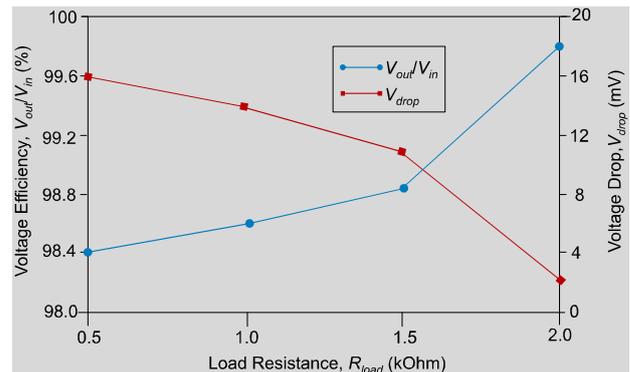

Fig. 12. Simulated voltage efficiency, Vout_dc/Vin_ac and voltage drop, Vdrop versus load resistance

It can be seen in Fig. 12, when Rload increased, the voltage efficiency increased while the voltage drop decreased leading to the efficient of CBR circuit. However, the changes of the voltage efficiency and voltage drop for variation Rload from 0.5 kΩ to 2.0 kΩ were minimal.

B. Measurement Results of CBR

For initial characterization purposes, a 50 Hz, 1.0 V amplitude sine wave from the function generator, Tektronix AFG 3252 is used as input ac source. The 0.5 kΩ load resistance is connected at the output of the CBR circuit.
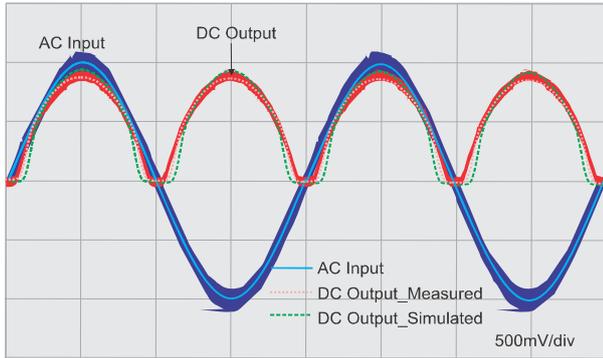
Fig. 13. Waveforms of the ac input and dc output voltages with resistive load

The performance of the CBR circuit is measured and compared with the simulated response as depicted in Fig. 13. It can be seen that the measured output voltage of the CBR is successfully rectified. The measu Furthermore, the output power of the CBR is varied with the output current. The output current range is measured from 0 to 1.8 mA. In Fig. 14, the measured output power of the CBR circuit was compared with simulated results. It can be seen that the measured output power is increased whilst the output current increased. With 1.0 kΩ of

resistive load, the output power of 1.22 mW is obtained for an output current of 1.272 mA. However, the different of the simulated and measured output power between the varied output current were minimal.red response shows the CBR circuit was reduced 2 % as compared to the simulation. The measured response shows good rectifying performance with only 40 mV of voltage drop which is 4 % less than the input voltage.
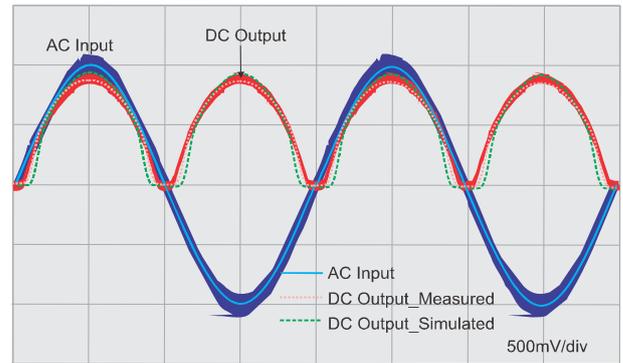

Fig. 14. Measured and simulated output power results versus output current for a 50 Hz and 1.0 V ac input.

TABLE 3: PERFORMANCE COMPARISON FOR CBR WITH AVAILABLE TOPOLOGIES AND TECHNOLOGIES OF CR FOR ENERGY HARVESTING APPLICATIONS

Previous Work	[5]	[6]	This Work
Technology	0.5 µm CMOS	0.35 µm CMOS	0.18 µm CMOS
Rectifier	Full Wave Rectifier	Negative Voltage Converter	Full Wave Bridge Rectifier (CBR)
P_O (W)	0.38 m	0.65 µ	1.22 m
V_{out_dc}/V_{in_ac} (%)	82.4	95	96
F_{in} (Hz)	20	200	50
A (mm^2)	0.013	0.007	0.0054

Table 3 above shows the performance comparison for the CBR circuit with available topologies and technologies of CR for energy harvesting applications. The CBR circuit is implemented into 0.18 µm CMOS process to reduce voltage drop, thus increasing the output power of the whole system. The CBR circuit implemented into 0.18 µm CMOS technology has highest output power compared to 0.5 µm and 0.35 µm CMOS technologies. For comparison, the CBR circuit achieves the output power of 1.22 mW at output current of 1.272 mA which is higher than performed in [5][6].

On the other hand, the CBR circuit has obtained the higher voltage efficiency. With 50 Hz and 1.0 V ac input magnitude, the CBR circuit obtains the voltage efficiency of 96 % which is higher than performed in [5].

Meanwhile, the performance of the CBR circuit has shown good reducing size which important for low power applications such energy harvesters. For comparison, the proposed bridge rectifier produced the active area of

0.0054 mm2, which is small other than produced in [5] by 58.5 % size reduction.

VIII. CONCLUSION

An input-powered AC/DC CMOS bridge rectifier (CBR) has been presented for low power applications using 0.18 µm CMOS technology. Using such technology, the threshold voltage can be reduced, which in consequence, minimizing the voltage drop. Also, the width, W of MOSFETs in the CBR circuit can be made large enough and the channel length, L to its minimum value, to increase the output power of the CBR circuit. The measured results of the proposed CBR with 1.0 V amplitude input at 50 Hz input frequency is obtained the voltage efficiency of 96 % with the output power of 1.22 mW which higher than performance in previous studies. Furthermore, substantial reduction of the overall size of the circuit can be observed in the CBR layout as

compared to other reported circuits. The topology, its design, and technique may be used for miniaturized applications such as micro-energy harvesters.

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