A Low Power Full-Swing Hybrid Full Adder using Modified GDI Cells

Bo Hong, Xiaoxia You, Jianping Hu*

Faculty of Information Science and Technology, Ningbo University, Ningbo, 315211, China

***Abstract* — A full adder is one of arithmetic cells is one of most important building block, which affects the performance of the whole digital system. In this paper, we present a new low power full-swing hybrid full adder using modified Gate Diffusion Input (GDI) techniques. The proposed hybrid full adder not only provides low power consumption but also high operating speed with full voltage swing at the output terminals. The simulations have been carried out by HSPICE in PTM45nm and 32nm technologies at different supply voltages. Performance comparisons with several traditional full adders including the conventional CMOS full adder, hybrid pass logic full adder with static CMOS output drive, and Hybrid-CMOS full adder show considerable improvements in terms of power dissipations and power delay product in low source voltages.**

Keywords - Low power; Gate diffusion input techniques; full adder; full swing; hybrid logic style

I. INTRODUCTION

With portable electronic product continuing to gain popularity, the performance demand for ICs is driving researchers to strive for lower power, higher speed and more reliability. The power dissipation is one of key problems when researchers design a digital system.

An adder is one of the most important and fundamental unit in arithmetic operation which is used widely in any digital systems, such as digital signal processing (DSP) and microprocessor. 1-bit full adder is a building block of adder operation, used in the critical path of complex arithmetic for multiplication, division and so on. Therefore, reducing power consumption in full adders would reduce the overall power consumption of the whole system. Enhancing the characteristics and performance of the 1-bit full adder is a significant goal and has attracted many attentions. An optimized design is required to prevent any reduction in the output signal swing, consume less power, have less delay in critical path and be reliable even at low supply voltage as manufacturing process scales towards nanometer.

II. GATE DIFFUSION INPUT TECHNIQUES

In order to reduce power consumption of circuits and complexity of circuit structure, the Gate Diffusion Input (GDI) technique is proposed by Alexander Fish in 2002 [1]. The GDI technology is based on the use of a basic GDI cell, which can successfully implemented only in twin-well CMOS or silicon on insulator (SOI) technologies. The researcher presented a modified GDI in 2010 [2]. The modified GDI cell is fully compatible for implementation in a standard CMOS process and presents reduced area, compared with the basic GDI cells.

At first glance, the modified GDI cell reminds one of the standard CMOS inverter, but there are some important differences. The modified GDI cell contains three inputs: *G* (common gate input of both NMOS and PMOS), *P* (input to the source of the PMOS), and *N* (input to the source of the NMOS), as shown in Fig. 1. It is shown that multiple Boolean functions can be implemented on the different input configuration by a modified GDI cell, as demonstrated in Table I.

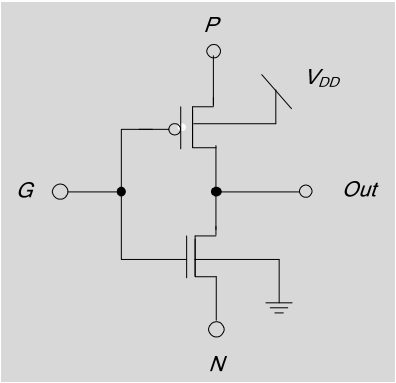


Figure 1. The circuit structure of modified GDI cell.

TABLE I. FUNCTIONAL TABLE OF MODIFIED GDI CELLS

N	*P*	*G*	*OUT*	Functional Table
0	*B*	*A*	$\overline{A}\cdot B$	F1
B	*A*	*A*	$\overline{A}+B$	F2
1	*B*	*A*	$A+B$	OR
B	*0*	*A*	$A\cdot B$	AND
C	*B*	*A*	$\overline{A}B+AC$	MUX
0	*B*	*A*	$\overline{A}$	NOT

The advantage of the circuits based on GDI cells are simpler structure, reduced number of transistors, and low

power dissipations. However, the output voltage may suffer from threshold voltage loss due to reduction of drive currents in GDI cell, and thus the output signal can not provide full swing output. The researchers have proposed various methods to restore output voltage. One of improved approach utilize special voltage restorer called as ULPD to reduce output voltage drop and create full swing output [3]. It also can use swing-restoration buffers with multiple threshold approaches [4]. Full swing GDI cell is proposed by using swing restoration transistors to improve the output swing when the threshold voltage drop may occur at the output [5].

III. REVIEWS FOR PREVIOUS FULL ADDERS

In recent years, many circuit structures have been proposed to implement 1-bit full adders. Each 1-bit full adder (FA) circuit has its own merits and demerits. These full adders can be divided into two main categories according to logic style: static logic style and dynamic logic style. The FA circuits based on static style are generally more reliable and less power, while dynamic logic style provides a high operation speed. We also can divide full adders into two groups based on characteristic of output swings: full swing full adder and non-full swing full adder. The advantage of full swing full adder is the good capability to operate reliable at a low supply voltage in deep sub-micrometer.

Various prior full swing full adders have been reported in literature [6-10]. The standard static CMOS full adder with 28 transistors, also called as conventional CMOS full adder (denoted as C-CMOS) is robust, but has high power dissipation. It has full-swing outputs and good driving capability due to the presence of inverters on the output node. It functions well at low supply voltages because it does not have threshold loss problem. However, large PMOS transistors in pull up network result in high power dissipations.

The transmission-gate full adder (TGA) uses transmission gates and inverters to implement XOR and multiplexing functions. The circuit has 20 transistors and can operate with full swing output voltage because these transmission gates can transmit both strong"1" and strong"0" signals. The transmission function full adder (TFA) only consists of 16 transistors by employing transmission functions. The advantages of TGA and TFA are low transistor count and lower power consumption compared with the standard static CMOS full adder. However, their performance degrades significantly because of poor driving capability when TGA or TFA are cascaded.

The other full adder, called as hybrid FA, utilize more logic styles than two different logic ones to realize logic functions. These designs exploit the features of different logic styles to build a low power full adder cell. Examples of hybrid FA are NEW-14T adder, hybrid pass logic with static CMOS output drive full adder (HPSC) [7], and Hybrid-CMOS full adder [8]. Some of these full adders are shown in Fig. 2 and Fig. 3.

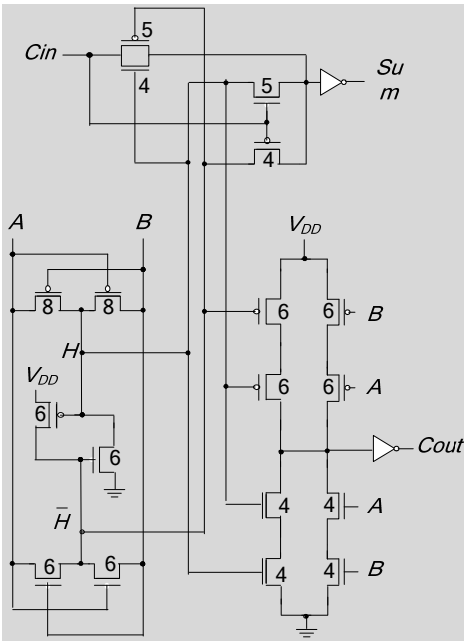


Figure 2. Hybrid pass logic with static CMOS output drive full-adder (HPSC).

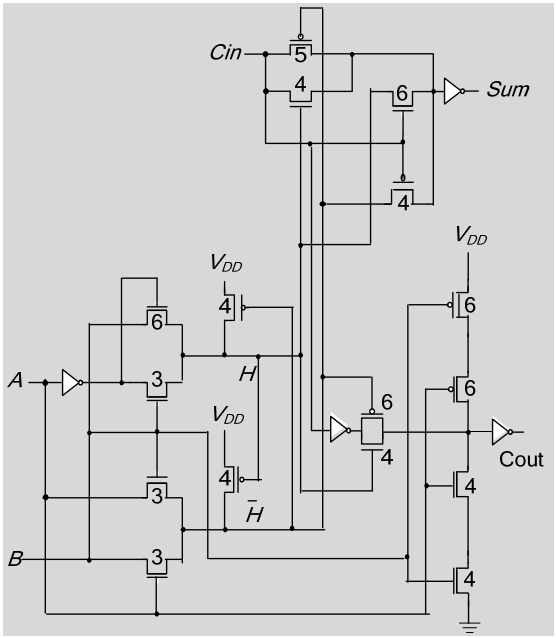


Figure 3. Hybrid-CMOS full adder (Hybrid-CMOS).

The HPSC full adder is designed by using pass transistor logic and static CMOS circuit design techniques. It needs 22 transistors. The drawback of the HPSC full adder is low operating speed, and is unsuitable for low supply voltage.

The Hybrid-CMOS full adder is implemented based on three logic style, complementary pass transistor logic, transmission gate logic, and static CMOS logic. The carry module of the Hybrid-CMOS full adder use static CMOS

logic in order to achieve enhanced performance and high driving capability. The transistor count of Hybrid-CMOS full adder is twenty-four. The power dissipation of the Hybrid-CMOS full adder is effectively reduced. However, The Hybrid-CMOS full adder is also unsuitable for low supply voltage as same as the HPSC full adder.

IV. Proposed Full-Swing Hybrid Full Adder Based on Modified GDI Cells

There are three input signals (*A*, *B*, *Cin*) and two output signals (*Sum*, *Cout)* in a full adder cell. The implementation of a full adder cell has many circuit structures because their output signals *Sum* and *Cout* can be expressed in many different logic expressions. We classify the different possible structures for a full adder cell into three broad categories based on their structures and logic expressions: XOR-XOR full adder, XNOR-XNOR full adder, and XOR-XNOR full adder.

In the category of XOR-XNOR full adder, the *Sum* and *Cout* outputs are generated by the expression (1) and (2), where *H* is exclusive or of two input *A* and *B* ($A \oplus B$), and $\overline{H}$ is exclusive nor $A \overline{\oplus} B$. The structure diagram of the XOR-XNOR full adder is comprised of three modules, which is shown in Fig. 4. Module 1 is a XOR-XNOR circuit producing and *H* and $\overline{H}$ signals, while the Module 2 and 3 are 2-to-1 multiplexers with *H* and $\overline{H}$ as select lines, which produce the signals of *Sum* and *Cout*. The HPSC full adder and Hybrid-CMOS full adder are examples of this category. In these types of adders, module 1 is a critical block because it can generate the *H* and $\overline{H}$ signals simultaneously.

$$Sum = A \oplus B \cdot \overline{C}_{in} + A \overline{\oplus} B \cdot C_{in} = H \cdot \overline{C}_{in} + \overline{H} \cdot C_{in} \quad (1)$$

$$Cout = A \overline{\oplus} B \cdot A + A \oplus B \cdot C_{in} = \overline{H} \cdot A + H \cdot C_{in} \quad (2)$$

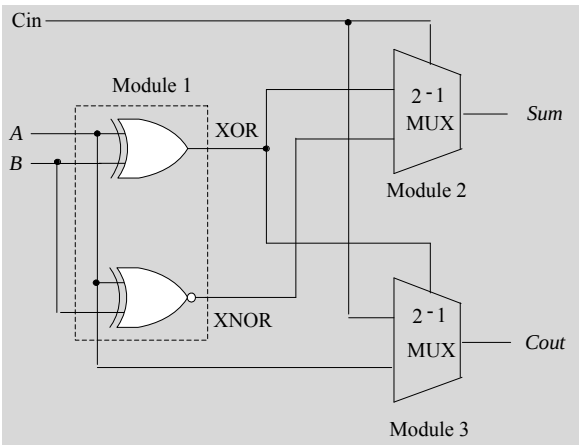


Figure 4. General structure of the XOR-XNOR full adder.

In recent years, more and more researchers proposed the circuit structures of simultaneous generation of full swing XOR and XNOR. The XOR-XNOR circuits based on pass transistor logic is presented in [7], shown as Fig 5. The circuit is consist of only six transistors and has a feedback connection between XOR and XNOR through adding one PMOS and one NMOS to improve the swing of output and driving capability.

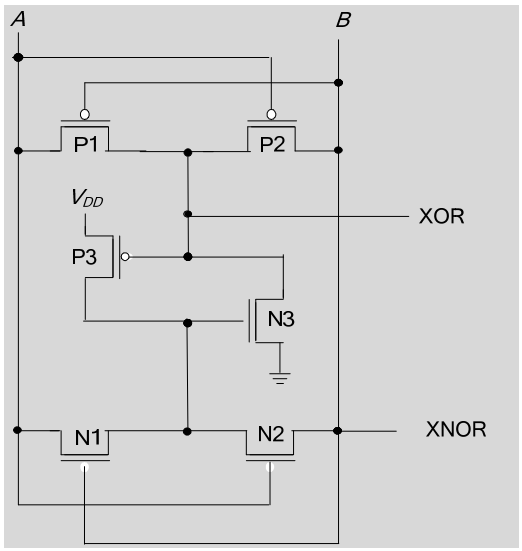


Figure 5. XOR-XNOR based on pass transistor logic in [7].

The circuit presented in [8] is shown as Fig. 6. It use complementary pass transistor logic to implement full swing XOR-XNOR circuit, where two cross-coupled pull-up PMOS transistors are added to the circuit to restore full-swing operation.

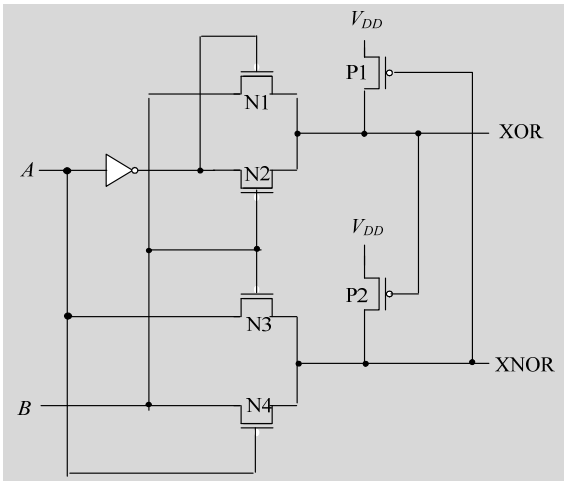


Figure 6. XOR-XNOR based on complementary pass transistor logic in [8].

The XOR-XNOR circuit can be implemented only with three modified GDI cells according to Fig. 1, as shown as Fig. **7**.This circuit structure is simple but its outputs are non full-swing because of threshold voltage drop problem.

We proposed a novel improved XOR-XNOR circuit based on modified GDI cells, as shown as Fig. 8, which uses ten transistors that generates XOR and XNOR full-swing

outputs simultaneously. The four transistors (P4, N4, P5, and N5) are added to provide feedback loop between two outputs to restore the output swing. This circuit not only can provide full swing operation but also can operate at low supply voltage.

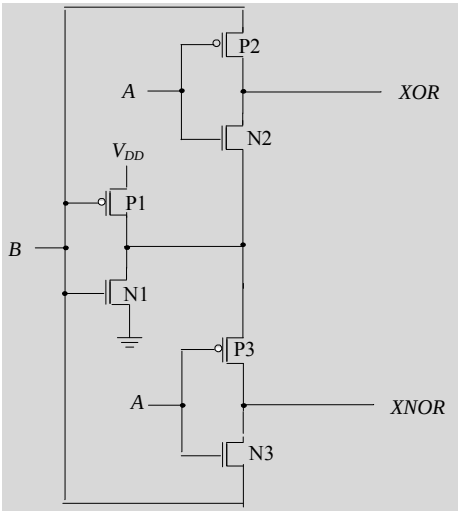


Figure 7. Non-full swing XOR-XNOR circuit based on GDI cell.

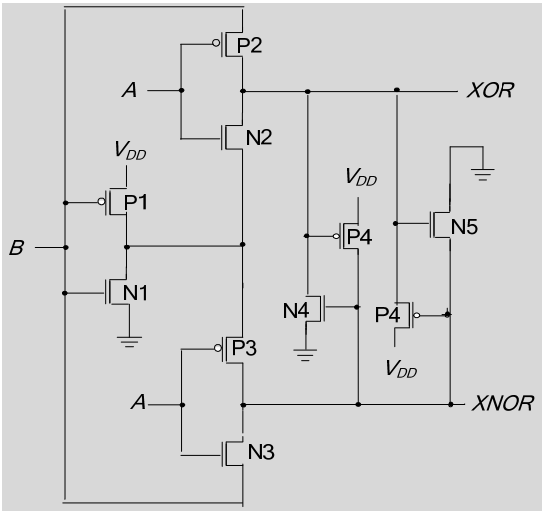


Figure 8. Proposed full swing XOR-XNOR circuit based on GDI Cell.

The performance of the proposed full swing XOR-XNOR circuit has been compared with the circuits in Fig. 5 and Fig. 6. The simulation results using HSPICE with 1V power supply voltage based on 45nm Technology are shown in Table II. We observed that the number of transistors in the proposed XOR-XNOR circuits is higher than the other two circuits but it consumes the least power dissipation. It is shown that the new circuit reduces the leakage consumption and short circuit consumption compared with the circuits in [7] and [8]. The proposed circuit not only consumes less power but also is 20% faster than the circuit in [7], and there is roughly 85% reduction in PDP. The propose circuit and the circuit in [8] have almost same speed but the new circuit consumes 3% less power dissipations.

TABLE II. SIMULATION RESULTS OF THE THREE XOR-XNOR CIRCUITS AT 45NM TECHNOLOGY WITH 100MHZ FREQUENCY AND 1V SOURCE VOLTAGE

Circuit Style	Circuit in [7]	Circuit in [8]	Proposed Circuit
Counts of Transistors	6	8	10
Power Dissipation (uw)	1.500	1.163	1.125
Delay (ns)	0.068	0.045	0.049
PDP	0.102	0.052	0.055
Improvement (PDP)	85%	-5%	1

The proposed full-swing hybrid full adder based on modified GDI cells (denoted as GDI-H) is shown in Fig. 9. For the new full adder, we use new XOR-XNOR circuit and two existing circuits in the three modules. The Module 2 uses transmission function logic to generate $\overline{Sum}$ and use static CMOS logic implement an inverter to generate *Sum*. This circuit has good driving capability and low PDP. The output *Cout* is obtained with two transmission gates.

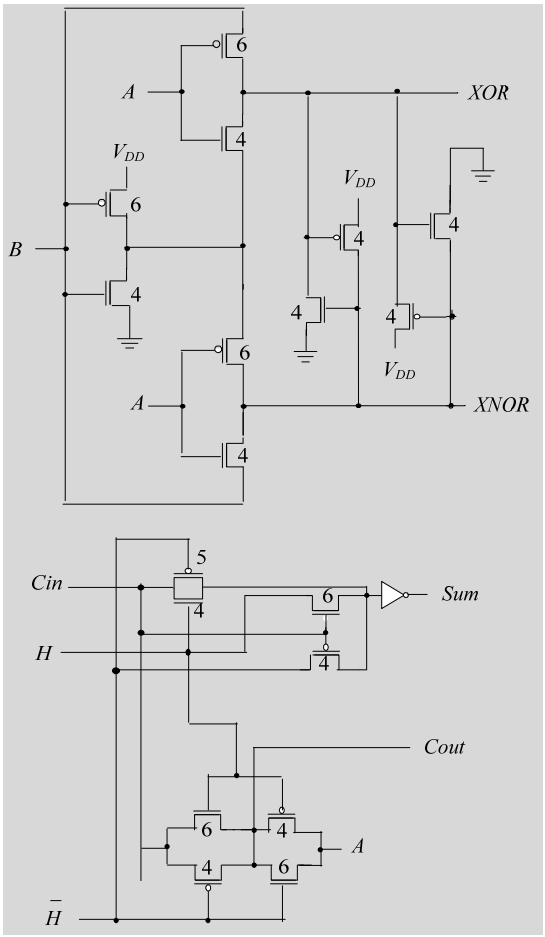
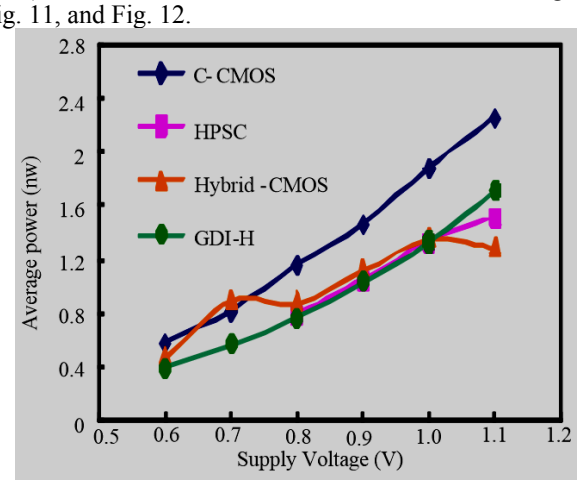


Figure 9. The proposed full swing hybrid full adder based on modified GDI cell (GDI-H).

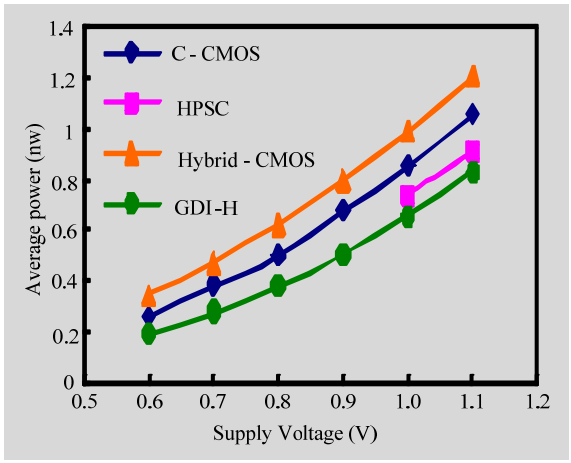
V. SIMULATIONS & COMPARISONS

In order to analyze the performance of the proposed circuit, HSPICE simulations were carried out based on PTM 45nm and PTM 32nm technologies, and its performances have been compared with the other three full swing full adders. The operating frequency of all the full adders is set at 200MHz. The average power consumption, worst-case delay and power delay products (PDP) are evaluated. The average power consumption is average value of circuit power consumption under consideration of all the possible input combinations and several cycles. The worst-case delay is chosen to maximum delay of all the transitions which is measured from 50% of the every input voltage swing to 50% of both the fall and rise edge at the output. Power delay product (PDP) has been calculated from production of worst-case delay and average power consumption.

The average power consumption, worst-case delay and PDP are evaluated under different supply voltages (0.6V-1.1V) for all the full adders and are summarized in Fig. 10, Fig. 11, and Fig. 12.



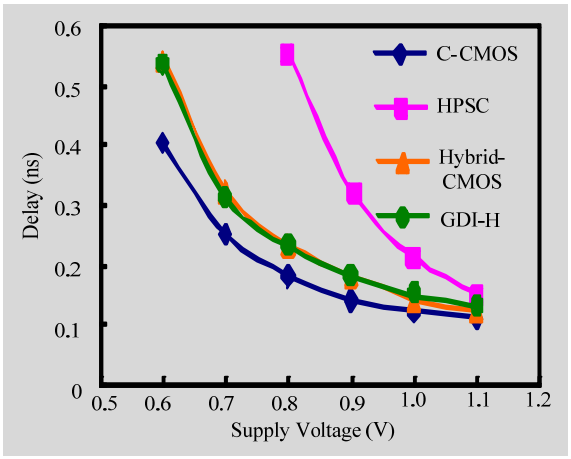
(a) PTM 45nm



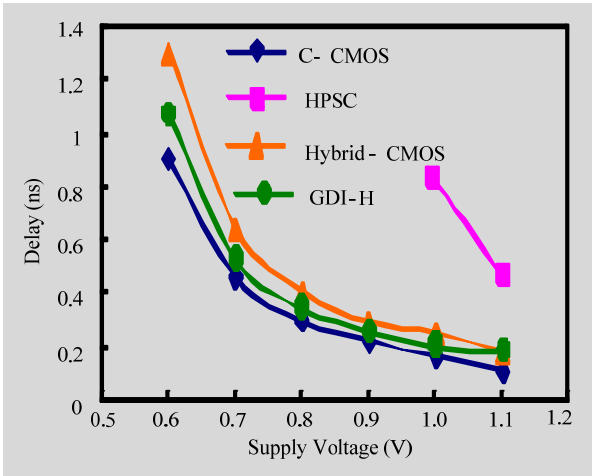
(b) PTM32 nm

Figure 10. Average power dissipations of the four full swing full adders in different supply voltages.

Clearly, the GDI-H full adder has the least power consumption at all varying supply voltages among four full adders. It is apparent that the C-CMOS has the smallest delay at lower supply voltage. The GDI-H full adder shows minimum delay at all supply voltages compared with HPSC and Hybrid-CMOS full adders. The HPSC full adder is unsuitable for low voltage operation because that it perform poorly under low voltage. The GDI-H full adder displays the best PDP characteristics for low supply voltage range.



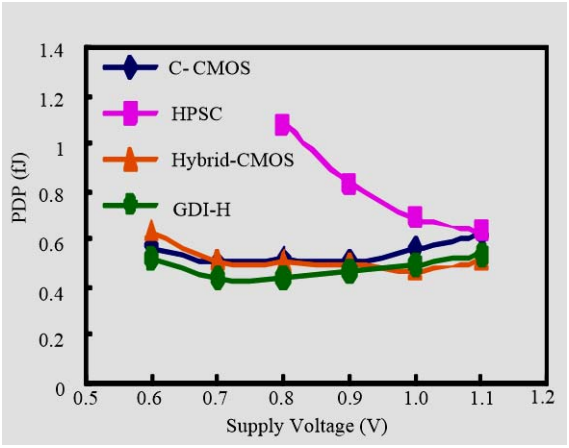
(a) PTM 45nm



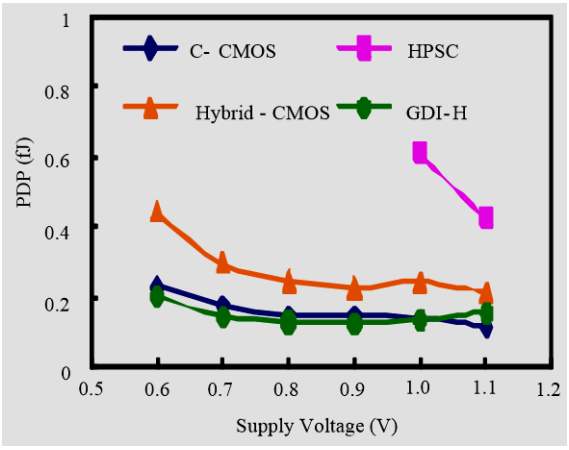
(b) PTM32 nm

Figure 11. The delay of the four full swing full adders in different supply voltages.

Table III shows the power consumption, propagation delay, PDP, and transistor counts of all four full adders with 0.8 V supply voltage and 200MHz operating frequency in PTM45 nm technology. The average power consumption of the GDI-H full adder is the smallest. Compared with the C-CMOS full adder, the new proposed adder consumes 40% less energy. There is roughly 20% reduction in PDP compared with the Hybrid full adder. Therefore, the GDI-H full adder is very suitable for low voltage operation.



(a) PTM45 nm



(b) PTM32 nm

Figure 12. The PDP of the four full swing full adders in different supply voltages.

TABLE III. SIMULATION RESULTS FOR THE PROPOSED FULL ADDER IN 45NM TECHNOLOGY AT 200MHZ FREQUENCY AND 0.8V SUPPLY VOLTAGE

FA	Counts of Transistors.	Average Power (nw)	Worst-case Delay (ns)	PDP (e^{-18})
C-CMOS	28	2.900	0.18	0.5220
HSPC	22	1.973	0.55	1.0849
Hybrid-CMOS	24	2.205	0.23	0.5072
GDI-Hybird	20	1.923	0.23	0.4422

VI. CONCLUSIONS

An adder is one of the most important and fundamental unit in arithmetic operation which is used widely in any digital systems, such as digital signal processing (DSP) and microprocessor. 1-bit full adder is a building block of adder operation, used in the critical path of complex arithmetic for multiplication, division and so on. Therefore, reducing power consumption in full adders would reduce the overall power consumption of the whole system.

In this paper, a novel low power full swing hybrid full adder using the GDI technique has been proposed. The new full adder not only provides low power consumption but also full voltage swing output. It performs well at low voltages with tremendous signal integrity and driving capability. Simulations have been performed by using HSPICE to evaluate the new full adder as well as three other adders, including C-CMOS, HPSC, and Hybrid-CMOS full adder. The simulation results show that the new full adder has minimum power consumption and PDP among four full adders for low supply voltage range.

ACKNOWLEDGMENT

This work was supported by the National Natural Science Foundation of China (No. 61671259, No. 61271137) and the Key Program of National Natural Science of China (No. 61131001).

REFERENCES

[1] A. Morgenshtein, A. Fish, and I. A. Wagner, "Gate-diffusion input (GDI)—a power-efficient method for digital combinatorial circuits, " IEEE Transactions on VLSI Systems, vol. 10, pp. 566-581, 2002.

[2] A. Morgenshtein, I. Shwartz, and A. Fish, "Gate diffusion input (GDI) logic in standard CMOS nanoscale process," in: Proceedings of IEEE Convention of Electrical and Electronics Engineers in Israel, pp. 776-780, 2010.

[3] V. Foroutan, M. Taheri, K. Navi, and A. A. Mazreah, "Design of two low power full adder cells using GDI structure and hybrid CMOS logic style," Journal of Integration, vol. 47, pp. 48-61, 2014.

[4] K. Dhar, "Design of a low power, high speed, energy efficient full adder using modified GDI and MVT scheme in 45nm technology," in: Proceedings of International Conference on Control, Instrumentation, Communication and Computational Technologies, pp. 36-41, 2014.

[5] A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, and A. Fish, "Full swing gate diffusion input logic case study of low power CLA adder design", Journal of Integration, vol. 47, pp. 62-70, 2014.

[6] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 10, pp. 20-29, 2002.

[7] M. Zhang, J. M. Gu, and C. H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in: Proceedings of International Symposium on Circuits and Systems, pp. 317-320, 2003.

[8] S. Goel, A. Kumar, and M. Bayoumi, "Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, pp. 1309-1321, 2006.

[9] S. Goel, S. Gollamudi, A. Kumar, and M. Bayoumi, "On the design of low-energy hybrid CMOS 1-bit full-adder cells," in: Proceedings of Midwest Symposium on Circuits and Systems, pp. 209-212, 2004.

[10] M. Kumar, M. A. Hussain, and L. L. K. Singh, "Design of a low power high speed ALU in 45nm using GDI Technique and its performance comparison," Computer Networks and Information Technologies, pp. 458-463, 2011.