Development of High Accuracy BiCMOS Current-Sensor and Error-Amplifier in Current-Mode DC-DC Boost Converter

Chan-Soo Lee* [1], Dae-Taek Chung [2]

[1] School of Electrical and Computer Engineering, Chungbuk National University, Cheong-Ju, Korea
* direct@chungbuk.ac.kr
[2] PNE SOLUTION CO., LTD., Suwon-si, Gyeonggi-do, Korea.

***Abstract* - This study aims at presenting a novel integrated BiCMOS amplifier and a current sensing circuit for a high accuracy and high performance DC-DC boost converter. A high gain amplifier and an accurately sensed inductor current are obtained in the feedback control circuit. The proposed current sensing circuit uses a simple current mirror instead of an op-amplifier as a voltage follower so that it can provide high accuracy without the reduction of power efficiency. The chip is fabricated from the 0.35 µm 2-poly 4-metal BiCMOS process. Bipolar transistor is applied to the current sources of the sensing circuit to obtain high current driving capability. The measurement shows that the current sensing circuit operates with an accuracy of higher than 92 % at the frequency of 50 KHz. The converter with a chip-size of 1 mm^2 operates at the output voltage of 4 ~ 7 V with minimum power consumption of 59mW. The HSPICE simulation results demonstrate the validity of both the current sensor and the error amplifier that are proposed in this study.**

Keywords - component; BiCMOS, boost converter, integrated, OTA, current-sensing circuit, current -mirror.

I. INTRODUCTION

The design of a high performance and high efficiency DC-DC boost converter has become important as battery-operated portable electronic devices are in great demand. Therefore, there is a need for high efficiency DC-DC boost converters, which are suitable for single-cell battery systems to minimize the physical size for portable devices and to maximize the operation time. Integrated DC-DC converters are essential components in power management ICs, efficiently providing power to all vital circuits of the battery powering block [1]-[3]. The DC-DC converter is normally composed of the power and feedback control blocks. Both voltage and current-mode controls are widely used in the DC-DC converter. Current-mode control is known to have advantages especially in terms of both stable operation and fast frequency response. Among the various elements in the control circuit of the current-mode DC-DC converter, a current sensing circuit and an error amplifier are crucial for the performance of the overall feedback control. Our work is focused on reducing chip-size without sacrificing high speed operation and power efficiency. The current-sensing circuit needs a low on-resistance transistor for a full swing operation of a low voltage integrated DC-DC converter. A bipolar transistor has lower on-resistance than MOSFET, whose switching time is faster [4, 5].

The reason for the application of the BiCMOS process in this paper is to meet the requirement for the low on-resistance transistors of the current-sensing circuit. The process is also applied to the differential pair and current sources of the error amplifier to obtain a fast transient response. The high on-resistance of MOS transistor helps interrupt this integrated boost converter with a supply voltage of 3 V so that the other transistors can operate properly, especially, in the current-sensing circuit which needs operating at it full capacity.

The voltage drop in the drain source of MOS transistors can cause other transistors to limit the mode of operation. Therefore, the bipolar transistor with lower on-resistance is a preferred device for the current sensing circuit.

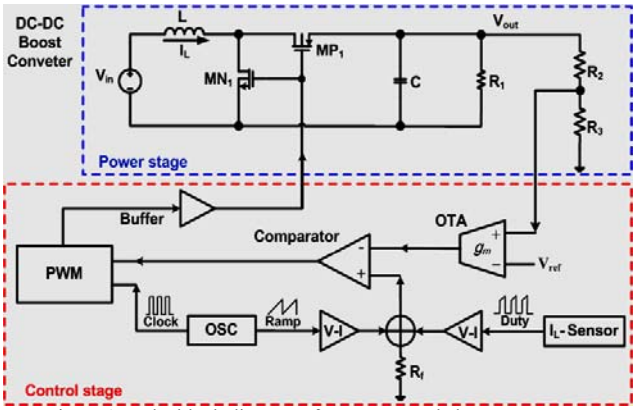

Figure 1. The block diagram of a current-mode boost converter.

Fig. 1 has the block diagram of a current-sensing circuit for current-mode boost converter. It is designed using a 0.35µm BiCMOS process. The advantage of BiCMOS technology is proposed in both the operational trans conductance amplifier(OTA) circuit and the current sensing circuit. These circuits are expected to provide superior performance in terms of high speed, high performance, low power consumption, and sensing accuracy. Fig. 1 shows the

structure of the converter which consists of power and feedback control stages. The power stage includes LC elements and two MOS switches (MP_1 and MN_1). Off-chip LC filter is designed with the inductance of 10 ~ 20mH and the capacitance of 100μF ~ 10 mF. The control stage is composed of current sensor, error amplifier, comparator, oscillator, V-I converter, pulse-width modulator (PWM), and buffer. This paper proposed that a current sensing circuit and error amplifier in the current mode DC-DC boost converter should be evaluated through BiCMOS process parameters. In Section II, the controller circuit used in the current-mode DC-DC boost converter is examined in detail. In Section III, the performance of the converter is assessed based on the simulation result. Finally, the conclusion of the paper is given in Section IV.

II. CIRCUIT IMPLEMENTATIONS

A. Error Amplifier Circuit:

A high-gain and wideband error amplifier is an essential requirement to make the most of the high switching frequency. The proposed error amplifier is designed to increase both the switching frequency and the fast transient response of DC – DC converters [6, 7].

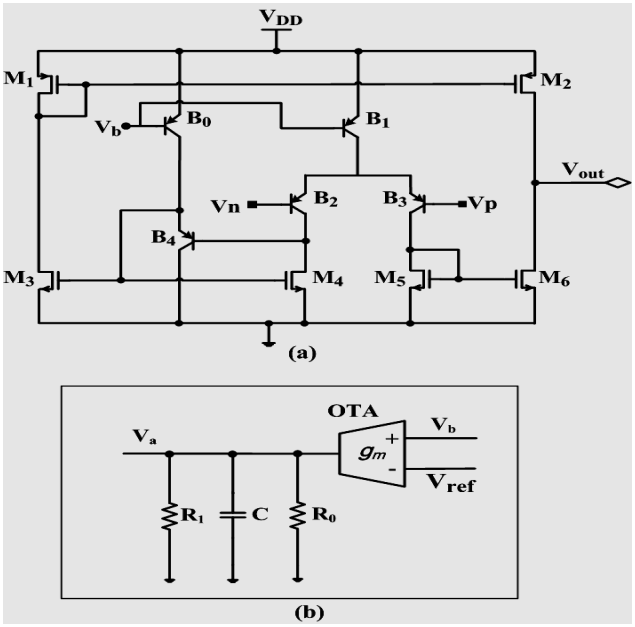

Figure 2. Schematic of (a) OTA circuit with (b) compensator circuit.

The proposed error amplifier in Fig. 2(a) is made up of input differential stage, output buffer, and bias circuit. This amplifier usually includes a compensation circuit to get the stability of both frequency response and fast response time. Poles and zeros are generated using the compensator, which yields a sufficient phase margin for a high stability. The current-mirror type OTA is composed of cascade bias, P-MOS differential-amplifier and source-follower. The differential-amplifier and the source follower help obtain high trans conductance and output resistance, which are the significant parameters for a stability of the phase margin in the frequency compensation. The control to output transfer function has two poles and can be written in the following form [8].

$$G_{(S)} = K\frac{1}{1+s\frac{L}{R}+s^2LC} \quad (1)$$

K, R, L, and C respectively indicates the constant, resistance, inductance, and capacitance in the power stage of the boost converter. The frequency response and stability are determined directly by their poles. We can determine if the converter circuit is stable by examining loop gain as a function of frequency. Fig. 3 represents OTA with compensator. Two resistors and a capacitor are used to generate another pole. The purpose of introducing a pole in the compensator is to provide a sufficient phase margin in the loop gain. The transfer function of the compensator is given as follows.

$$A_{(S)} \cong g_m R_0 \frac{1}{1+sR_0C_1} \quad (2)$$

In the function, R_o is the output resistance and g_m is the trans-conductance of the OTA. When the compensator resistance, R_1, is much smaller than the output resistance, the output resistance in the transfer function can be switched to R_1. The size limitation of capacitor in an integrated circuit causes the pole in the compensator to mostly depend on the resistance in an effort to improve the stability of the converter circuit. The loop gain depends on the multiplication of equations above: (1) and (2). As mentioned above, the purpose of introducing a pole in the compensator is to supply a sufficient phase margin in the loop gain. When the pole in the compensator is located on the left side of the poles of Eq. (1), the phase margin is usually increasing, which can help obtain more stability.

B. Current Sensing Circuit:

Fig. 3 shows the proposed BiCMOS current sensing circuit. The circuit requires an operational amplifier as a voltage follower [1, 2]. The amplifier causes some undesirable problems such as die area, sensing speed, and power consumption. Moreover, the accuracy of the sensing circuit is degraded due to the finite gain of amplifier. In the sensing circuit using an operational amplifier, a feedback loop exists across the amplifier and unstable oscillation can be possible in the frequency response. The aspect ratio of the power MOSFET to the sensing transistor is K = 500 in this design, which helps reduce the power consumption in the sensing FET.

A current mirror instead of an amplifier is introduced as a voltage follower in the current sensing circuit [3, 9]. The

proposed current sensing circuit does not need an operational amplifier as a voltage follower. The structure uses a fewer transistors, which can help reduce the power consumption. In this structure, it is possible to realize an on-chip BiCMOS current sensing circuit. The current sensing FET N_5 is in parallel with the power MOSFET N_1. The application of the sensing FET, which measures the current in the power MOSFET, needs a current mirror to act as a voltage follower. The matched currents can simply be attained by the aspect ratios between the MOS transistors, which enables the high accuracy of the sensing circuit with low supply power.

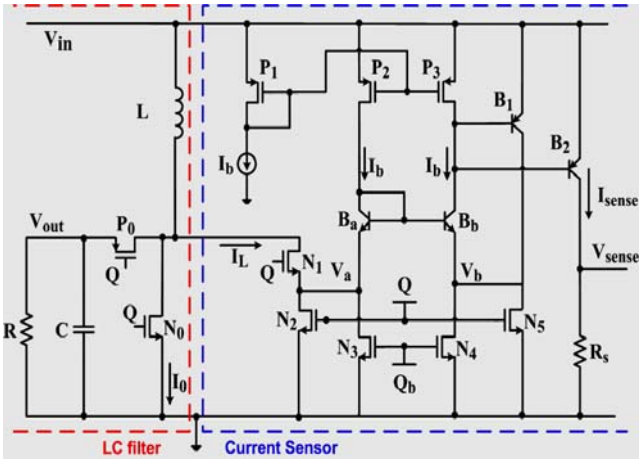

Figure 3. The block diagram of a current-mode boost converter.

As shown in Fig. 3, the voltage follower consists of two bipolar transistors: B_a and B_b. These two bipolar transistors, B_a and B_b are matched and are biased in the saturation region. The voltage V_a, which is the emitter voltage of the bipolar transistors B_a, is almost the same as the voltage V_b. The voltage follower keeps the node voltages the same as bipolar current sources that waste no static power. By the applications of voltage follower and current mirror inside the sensing circuit, the scaled inductor current can be matched to the sensing current I_{sense}. During the sensor on state, the power MOSFET and sensing FET are turned on and their drain source voltages are almost the same. The sensing current, I_{sense} is almost the same as the drain current of the transistor N_2. The aspect ratio between the power MOSFET N_1 and sense FET N_5 is adjusted to 500 to reduce the power consumption in the sensing FET.

During the ON period of the current sensing circuit shown in Fig. 4 (a), power MOSFET P_0 is turned off by setting V_Q high, while other transistors, N_1 and N_2 are turned on. Since the voltage follower provides V_a and V_b same, the drain current of the transistor N_2 is mirrored to the transistor N_5. The transistor N_2 and sense FET N_5 have the same gate and drain voltages, the drain currents of the transistors will depend on the aspect ratio of the channels.

The power MOSFET N_1 and the other transistors N_2, N_3, and N_4 are scaled so that the drain current on the sensing side is much smaller as compared to the output current I_{out}, which passes through the power MOSFET N_1. The scaled inductor current is the sensing current I_{sense} passing through the sensing resistor R_S. The current sensor has a negligible effect on the energy storage in inductor. As K is the aspect ratio between the MOSFET N_2 and N_5 transistors, the resistance of the MOSFET N_2 is K times the resistance of the transistors N_1 or N_2. Therefore, the drain current in the transistor N_2 can be written as $I_0 = K (I_1 + I_2)$, where I_1 and I_2 are the currents in the transistors N_1 and N_2. As the drain current I_1 is the same as I_b, where the bias current I_b is quite small, the current I_2 can be written as $I_2 = I_1/K + I_b$.

On the other hand, the drain current I_5 in the transistor N_5 is same with I_2 because of the voltage follower. Eventually, the sensing current I_{sense} flowing through internal resistor R_S is the scaled inductor current[I_1/K], which is quite smaller than the inductor current during the ON period.

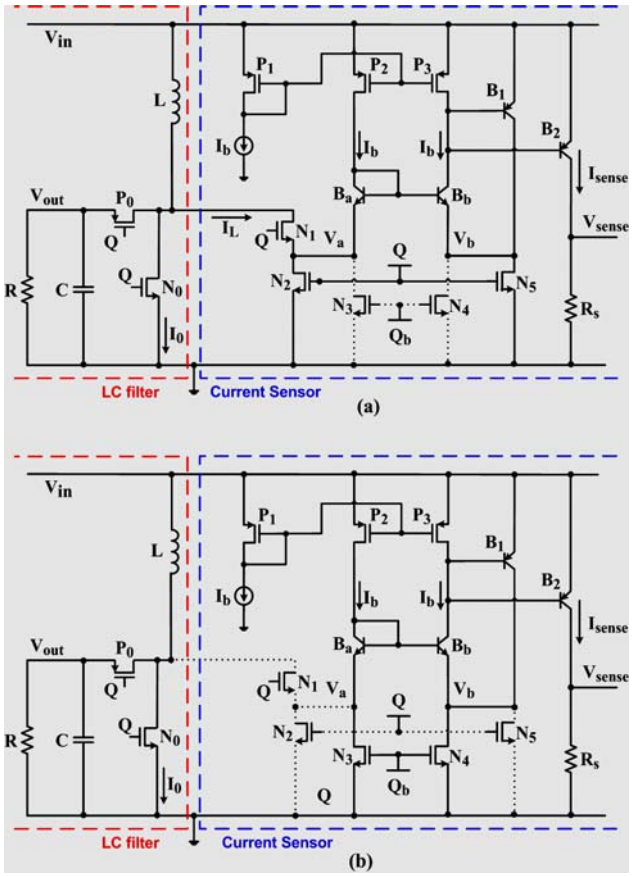

Figure 4. Current-sensing circuit during the (a) ON period and (b) OFF period.

During the OFF period of the current-sensing circuit shown in Fig. 4 (b), MOS transistors N_1, N_2, and N_5 are turned off. Switches N_3 and N_4 are turned on, and their drain currents are the same as the bias current, I_b. in Fig. 4 (b) are turned off by setting V_Q low, while PMOS transistor P_0 is

turned on. The inductor discharges through the transistor P_0 and the inductor current has a negative slope during the discharge. The current through the transistors, P_2 and P_3 is almost the same with I_b, which is a small bias current. The sensing current I_{sense} through the BJT B_2 is also the same small current. The sensing current during the OFF period is a negligible current compared to that during the ON period. As the sensed inductor current is scaled down, the power loss in the sensing circuit is significantly reduced. The accuracy of the sensed inductor current is dependent on the current mirror of MOSFET N_2 and N_5 in Fig. 4 and the resistor, R_{sense}, is stated in the equation. An op-amp is used as a voltage mirror so that the sensing current, I_{sense}, is matched to the inductor current, I_L. The sensing signal, V_{sense}, is given by:

$$V_{sense} = I_{sense} R_{sense} = \frac{I_L}{500} \quad (3)$$

The accuracy of the sensed inductor current relys on the MOSFET N_2, the sensing FET N_5, and the sensing resistor, R_S. The resistor R_S allows converting the current signal to a voltage signal so that V_{sense} is proportional to the sensing current.

III. RESULTS

The current-mode DC-DC boost converter has been designed in 0.35μm BiCMOS technology with 2-poly and 4-metal process. The converter's layout is shown in Fig. 5. The chip area is about 1mm^2.

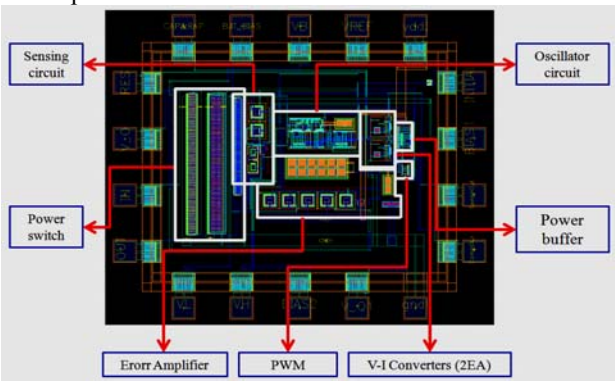

Figure 5. Layout of DC-DC boost converter.

The transient time is about 4 μsec at the frequency of 250 KHz and the supply voltage of 3.5 V. With variation of frequency and supply voltage, it was within 10 μsec. This indicates that the proposed circuits of the error amplifier, compensator, and comparator work fast and properly in the integrated DC-DC control circuit.

The stability of the control circuit is analyzed in terms of gain and phase margins. Fig. 6 shows the frequency characteristics of the output of error amplifier which has poles due to the natural frequency of LC filter and the compensation frequency which comes from the equations (1) and (2). The frequency characteristic of the compensated error amplifier is combined into the control feedback loop characteristics of the DC-DC boost converter. The effects of the amplifier gain on the stability are examined with the same poles, where the natural and compensator frequencies are 0.4 KHz and 16 KHz respectively. The gains of (M) and (N) in Fig. 6 are about 20 and 40 dB respectively.

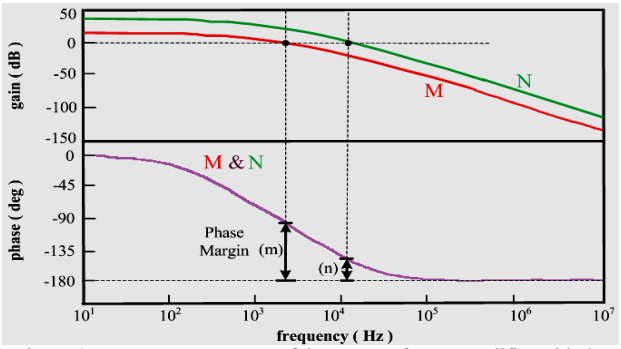

Figure 6. Frequency response of the output of error amplifier with the difference of the gain in amplifier, (M) 16 dB and (N) 37 dB.

The frequency response in Fig. 6 shows the phase margin of 85° in (M) and 25° in (N). The optimal phase margin is over 60°. The result indicates that the higher gain in current mode DC-DC boost converter can be reduce the phase margin and provide unstable condition into the frequency response although the higher gain in the amplifier provides fast transient response and a low quiescent current. The designed error amplifier maintains a low quiescent current during the normal operation and can be endurable to the large signal variation. In order to maintain the stability of the converter, the trans conductance of the error amplifier is well controlled into our work.

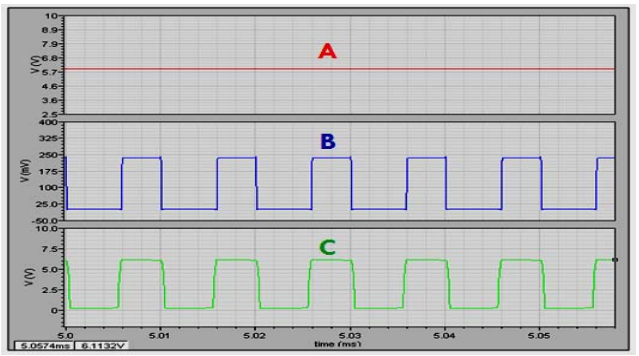

Figure 7. Simulation result of the current ensing circuit, (A) output voltage, (B) sensing signal, and (C) inductor voltage V_x.

Fig. 7 showing the output voltage (A), sensing voltage (B), and inductor voltage V_x (C) in the sensing circuit. The simulation result is obtained at the input voltage of 2.5 V and the switching frequency of 50 KHz. In the sensing circuit in Fig. 3, BJT is used for the current source and the voltage follower, thus providing a larger current and a smaller on-resistance that is possible with a conventional MOS transistor circuit. The inductor voltage V_x is measured

after the inductor in the current sensing circuit of Fig. 3, where the switching transistors, P_0, N_0, N_1, and N_2 are operated by the low and higher logic state V_Q. The simulation result of the sensing current from the output voltage (A) is about 6 V and the ripple ratio is within 3%. The minimum power consumption of the converter is about 35mW. The sensing signal (B) is almost identical to the inductor current by the ratio 500 between the power MOSFET and sense FET, corresponding to 35μA with the inductor current of 300mA, which means the sensing accuracy is 95 %.

The simulation result of the sensing voltage with different duty ratio is shown in Figure 8. For an inductor current of 150 mA, the sensing current of 0.3 mA should be obtained by considering the aspect ratio between the power and sense FETS. The sensing currents with different duty ratios are found to the sensing inductor current accurately.

At the boundary between discontinuous and continuous conduction also depends on other parameters such as inductance in LC filter and frequency.

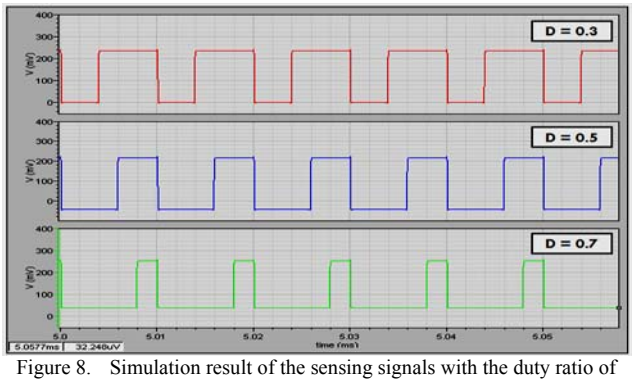

Figure 8. Simulation result of the sensing signals with the duty ratio of 0.3, 0.5 and 0.7.

Table 1 summarizes the performance of the designed converter. The proposed boost converter achieves the high figure of merit with a small chip area.

TABLE 1. PERFORMANCE COMPARISON OF DC-DC BOOST CONVERTERS.

Ref.	[1]	[2]	This work
Switch - mode	Boost	Boost	Boost
Process	CMOS 0.6 μm	BiCMOS 0.35 μm	BiCMOS 0.35 μm
Freq.(MHz)	0.1	0.01 ~ 0.1	0.01 ~ 0.1
Vin (V)	1 ~ 3.	3	3
Vout(V)	1.5 ~ 2.5	4.8 ~ 8	4 ~ 8
Size (mm^2)	2.5	1.5	1
Efficiency	Max 95.5%	84%	92% (Sim.)
Load Current (mA)	10 ~ 150	5 ~ 150	4 ~ 150

IV. CONCLUSION

A high performance BiCMOS technology is applied to the error amplifier and current-sensing circuit for the DC-DC boost converter. The simulation results show the performances of both the proposed OTA circuit and the current sensing circuit. This current sensing circuit will be useful for power electronic and telecommunication technology.

A high and low power current sensing circuit is introduced for the high performance DC-DC boost converter. The proposed current sensing circuit doesn't use op- amplifier, therefore low power consumption and high sensing speed can be achieved. Furthermore, the sensing signal is exactly proportional to the inductor current and doesn't contain the offset-current thus, it can offer a higher current sensing performance than the existing current sensing circuit. The proposed BiCMOS current sensing circuit is applied to the sensing circuit in order to obtain low on-resistance transistors. In the proposed error amplifier, BJT differential amplifier with cascode transistors are used to have a high gain and stable frequency response. The simulation results of the sensing current and the output voltage are obtained as expected in the 2-poly 4-metal 0.35μm BiCMOS process. The sensing circuit operates with an accuracy of 95% under power consumption of 37 mW.

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